Code No: R05320402 **Set No. 1**

III B.Tech II Semester Regular Examinations, Apr/May 2008
VLSI DESIGN
(Common to Electronics & Communication Engineering, Bio-Medical Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Describe the two commonly used methods for obtaining integrated capacitor. [16]

2. (a) Explain various regions of CMOS inverter transfer characteristics.
   (b) For a CMOS inverter, calculate the shift in the transfer characteristic curve when β_n/β_p ratio is varied from 1/1 to 10/1. [8+8]

3. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
   (b) What are the effects of scaling on V_t?
   (c) What are design rules? Why is metal metal spacing larger than poly -poly spacing. [8+4+4]

4. Calculate the rise time and fall time of the CMOS inverter $(W/L)_n$= 6 and $(W/L)_p$=8, K'_n =150μ A/V^2, V_{tn} =0.7V,K'_p= 62 μ A/V^2, V_{tp}=-0.85V , V_{DD} =3.3V. Total output capacitance =150 fF. [16]

5. (a) Explain the CMOS system design based on the data path operators with a suitable example.
   (b) Draw and explain the basic Memory- chip architecture. [8+8]

6. (a) Draw the typical standard-cell structure showing low-power cell and explain it.
   (b) Sketch a diagram for two input XOR using PLA and explain its operation with the help of truth table. [8+8]

7. (a) Write a VHDL Program for a divide-by-3 counter with suitable state diagram.
   (b) Compare all available design verification tools. [8+8]

8. (a) Explain how an improved layout can be reduced faults in CMOS circuits.
   (b) Explain how a pseudo random sequence generator may be used to test a 16-bit data path. How would the outputs be collected and checked. [6+10]

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Code No: R05320402 **Set No. 2**

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VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. With neat sketches, explain in detail, all the steps involved in electron lithography process. [16]

2. (a) Explain nMOS inverter and latch up in CMOS circuits?
   (b) Draw the nMOS transistor circuit model and explain various components of the model. [8+8]

3. Draw the stick diagram and mask layout for a CMOS two input NOR gate and stick diagram of two input NAND gate. [16]

4. (a) Explain the concept of sheet resistance and apply it to compute the ON resistance (V_{DD} to GND) of an NMOS inverter having pull up to pull down ratio of 4:1, If n channel resistance is $R_{sn} = 10^4\ \Omega$ per square.
   (b) Calculate the gate capacitance value of 5μm technology minimum size transistor with gate to channel capacitance value is $4 \times 10^{-4} pF/\mu m^2$. [10+6]

5. (a) Explain the CMOS system design based on the data path operators with a suitable example.
   (b) Draw and explain the basic Memory- chip architecture. [8+8]

6. (a) What are the characteristics of 22V10 PAL CMOS device and draw its I/O structure.
   (b) Explain any one chip architecture that used the antifuse and give its advantages. [8+8]

7. (a) What are the different types of operators used in VHDL? Give some examples using this.
   (b) Compare the Circuit-level, Logic-level, switch-level and Timing simulations. [8+8]

8. (a) compare functionality test and manufacturing test.
   (b) What type of testing techniques are suitable for the following:
      i. Memories
      ii. Random logic
      iii. Data path.
   (c) How IDDQ testing is used to test the bridge faults? [5+6+5]

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Code No: R05320402 **Set No. 3**

III B.Tech II Semester Regular Examinations, Apr/May 2008
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**
Answer any FIVE Questions
All Questions carry equal marks
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1. (a) What is Moore's law? Explain its relevance with respect to evolution of IC Technology.
   (b) What is the size of silicon wafer used for manufacturing state-of-the art VLSI ICs?
   (c) What is the minimum feature size of current commercial VLSI devices?[8+4+4]

2. Compare the relative merits of three different forms of pull up for an inverter circuits. What is the best choice for realization in
   (a) nMOS technology
   (b) CMOS technology. [16]

3. Draw the stick diagram and a translated mask layout for nMOS inverter circuit. [16]

4. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [16]

5. (a) Compare the different types of CMOS subsystem Multipliers.
   (b) Design a schematic for an 8-word × 2-bit NAND ROM that serves a lookup table to implement a full adder. [8+8]

6. (a) Explain the methods of programming of PAL CMOS device.
   (b) Draw and explain the architecture of an FPGA . [8+8]

7. (a) What are the different data types available in VHDL and how they are indicated?
   (b) Write a VHDL program for a 4-bit Counter with Asynchronous reset. [8+8]

8. (a) Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
   (b) Draw the state diagram of TAP Controller and explain how it provides the control signals for test data and instruction register. [8+8]

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Code No: R05320402 **Set No. 4**

III B.Tech II Semester Regular Examinations, Apr/May 2008
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the following:
   (a) Thermal oxidation technique
   (b) Kinetics of thermal oxidation. [8+8]
2. (a) Explain the operation of BiCMOS inverter? Clearly specify its characteristics.
   (b) Explain how the BiCMOS inverter performance can be improved. [8+8]
3. Explain the following
   (a) Double metal MOS process rules.
   (b) Design rules for P- well CMOS process. [8+8]
4. (a) Define and explain the following:
      i. Sheet resistance concept applied to MOS transistors and inverters.
      ii. Standard unit of capacitance.
   (b) Explain the requirement and functioning of a delay unit. [4+4+8]
5. (a) Draw the schematic for tiny XOR gate and explain its operation.
   (b) Draw the circuit diagram for 4-by-4 barrel shifter using complementary transmission gates and explain its shifting operation. [8+8]
6. (a) Explain the function of 4:1 Mux in PAL CMOS device with the help of I/O structure.
   (b) Explain how the pass transistors are used to connect wire segments for the purpose of FPGA programming. [8+8]
7. (a) What are the advantages of Hardware Description Languages and give some examples?
   (b) Explain the different types of simulators used to predict and verify the performance of given circuit. [8+8]
8. (a) Draw the basic structure of parallel scan and explain how it reduces the long scan chains.
   (b) Draw the state diagram of TAP Controller and explain how it provides the control signals for test data and instruction register. [8+8]

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