Code No: RT31041 **R13** SET - 1

III B. Tech I Semester Regular Examinations, November- 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

*****

PART –A

1	a)	Define storage time and transition time of a diode.	[3M]
	b)	What are the advantages and disadvantages of a direct coupled binary?	[4M]
	c)	What do you mean by phase jitter?	[3M]
	d)	State and prove clamping circuit theorem.	[4M]
	e)	What do you mean by Schotty TTL? Why is it faster than standard TTL?	[4M]
	f)	What does the display of a sampling scope consists of?	[4M]

PART -B

2	a)	Prove that a low pass circuit acts as an integrator. Derive an expression for the output voltage levels under steady state conditions of a low pass circuit excited by a ramp input.	[8M]
	b)	Explain RLC ringing circuit with a neat sketch.	[8M]
3	a)	Define i) Rise time ii) Fall time iii) Delay time iv) Storage time Explain the factors which contribute to the delay time of transistor.	[8M]
	b)	Draw the circuit of CMOS NOR gate and explain its operation. Mention the advantages of CMOS over the other digital logic families.	[8M]
4	a)	Describe the sequence of events in an n-p-n transistor to change from cutoff to saturation and vice versa. How does temperature affect the saturation junction of a transistor?	[8M]
	b)	Draw and explain the circuit diagram of integrated positive TTL AND & OR gates.	[8M]
5	a)	Explain the operation of a Monostable multivibrator and derive for the pulse width with necessary waveforms & circuirts.	[8M]
	b)	Design a collector coupled astable multivibrator using NPN silicon transistors with h_{fe}=40, r_{bb}=200Ω supploied with Vcc=10V and circuit component values are Rc=1.2KΩ and C=270 pF.	[8M]
6	a)	Explain the working of a transistor Bootstrap sweep circuit and derive expression for the slope sweep error.	[8M]
	b)	Why the time base generators are called sweep circuits? Give most important applications of time –base generators.	[8M]
7	a)	Explain how the loading of the control signal is reduced when the number of inputs increases in a sampling gate.	[8M]
	b)	Draw and explain the waveforms of a frequency division by an Astable multivibrator.	[8M]

*****

||''|'''|''|'|'''||

Code No: RT31041 **R13** SET - 2

III B. Tech I Semester Regular Examinations, November - 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**

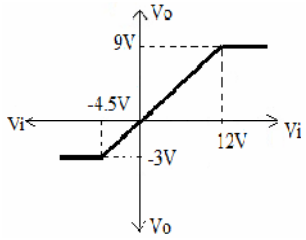
*****

PART –A

1	a)	What are the reasons for existence of rise time and fall time?	[4M]
	b)	Why a monostable multivibrator is also called a delay circuit? Explain.	[3M]
	c)	What do you mean by synchronization on a one-to-one basis and that with frequency division?	[4M]
	d)	Which logic gates are suitable for wired OR operations and why?	[3M]
	e)	What do you mean by pedestal? What are the advantages of diode sampling gates?	[4M]
	f)	What is hysteresis how it can be eliminated in a Schmitt trigger?	[4M]

PART -B

2	a)	Draw the output waveform of an RC high-pass circuit with a square wave input under different time constants. Derive the expression for percentage of tilt.	[8M]
	b)	Draw a Schmitt Trigger using transistors and derive for UTP & LTP.	[8M]
3	a)	Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics	[8M]
	b)	State and prove clamping circuit theorem.	[4M]
	c)	The ideal transfer characteristic of particular clipper circuit is shown in Figure.2. Design the circuit using ideal diodes and draw the input-output waveforms with proper explanation, if Vi = 15 Sin ωt.	[4M]



4	a)	Explain with the help of suitable waveforms the switching times of a diode switch. Derive the expression for reverse recovery time.	[8M]
	b)	Draw and explain the circuit diagram of integrated positive RTL NOR gate.	[6M]
	c)	Explain the reason for delay transition in a transistor as a switching element.	[2M]
5	a)	Design and draw a collector-coupled ONE-SHOT using silicon npn transistors with $h_{FE(min)}$ =20. In stable state, the transistor in cut-off has V_{BE} = -1V and the transistor in saturation has base current, I_B which is 50% excess of the $I_{B(min)}$ value. Assume VCC = 8V, IC(sat) =2mA, delay time = 2.5ms & $R_1 = R_2$. Find R_C, R, R1, C and V_{BB} .	[8M]

||''|'''|''|'|'''||

b) Draw the circuit diagram of an astable multivibrator and obtain all the steady state voltages and currents. Show how it acts as a voltage to frequency converter. [8M]

6 a) What are the different methods of generating time-base waveforms? Explain about each briefly. [8M]

b) Explain the working of Transistor Miller sweep circuit. What are its advantages over Bootstrap sweep circuits? [8M]

7 a) With the help of a neat circuit diagram and waveforms, explain the method to achieve frequency synchronization using pulse train as sync signals. [8M]

b) Explain the function of a sampling gate used in Sampling Scopes also explain how sampling gate is used in chopping amplifiers. [8M]

*****

||''|'''|''|'|''''||

Code No: RT31041 **R13** SET - 3

III B. Tech I Semester Regular Examinations, November - 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

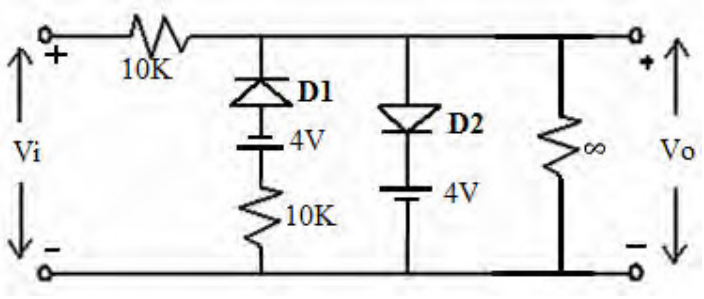
Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
*****

PART –A

1	a)	What is direct coupled binary? Give its advantages and disadvantages.	[4M]
	b)	What do you mean by blocked condition in astable multivibrator?	[3M]
	c)	How is the deviation from linearity expressed?	[3M]
	d)	What do you mean by synchronization? When do we say two waveform generators are synchronized?	[4M]
	e)	What are the advantages of MOS families over bipolar families?	[4M]
	f)	What are the advantages and disadvantages of unidirectional diode gates?	[4M]

PART -B

2	a)	Derive an expression for the output of low pass RC circuit excited by a step input. Draw the output for different time constants.	[8M]
	b)	What is an attenuator? How can an uncompensated attenuator be modified as a compensated attenuator. Give the comparison between perfect compensation, under compensation and over compensation.	[8M]
3	a)	Explain the working of a two-level diode clipper with the help of circuit diagram, waveform and transfer characteristics.	[6M]
	b)	Determine the output waveform for the biased clipping circuit for the square wave input.	[6M]
	c)	A voltage signal of (10 Sinωt) is applied to the circuit with ideal diodes shown in figure below. Estimate the maximum & minimum values of output waveform and maximum current through each diode. Also draw the input-output waveforms with proper explanation	[4M]



||''|'''|''|'|'''||

4 a) Briefly discuss the influence of breakdown voltages on the choice of supply voltage in a transistor switch. [4M]

b) Explain the characteristics and implementation of the following digital logic family i) CMOS, ii) ECL [8M]

c) Classify the basic families that belong to the bipolar families and to the MOS families. [4M]

5 a) b) Design a Schmitt trigger circuit using npn silicon transistors with V_{BE} = 0.7V, $V_{CE}(sat)$ = 0.2V, $h_{fe}(min)$ = 60 and $I_C(ON)$ = 3mA to meet the following specifications: V_{CC} =12V, upper threshold voltage, V_{UT} = 4V, lower threshold voltage, V_{LT} =2V. [8M]

b) What are transpose capacitors? Explain how the commutating capacitors will increase the speed of a fixed-bias binary. [8M]

6 a) Define and derive the terms slope error, displacement error and transmission error. [8M]

b) Explain the basic principles of Miller and Bootstrap time-base generators. Give the comparison of both the generation methods. [8M]

7 a) What is synchronization? Why it is necessary in waveform generators? Explain the synchronization of a sweep circuit with symmetrical signals. [8M]

b) Explain how to cancel the pedestal in a sampling gate with suitable circuit diagram. [8M]

*****

||''|'''|''|'|''''||

Code No: RT31041 **R13** SET - 4

III B. Tech I Semester Regular Examinations, November - 2015
PULSE AND DIGITAL CIRCUITS
(Common to ECE and EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
*****

PART –A

1	a)	Which signal can preserve its wave shape when transmitted through a linear network and explain how it can.	[4M]
	b)	Show the relationship between the percentage of tilt and cutoff frequency for a high pass RC circuit.	[3M]
	c)	What are the applications of time base generators?	[3M]
	d)	What is non-saturated binary? What are its drawbacks?	[4M]
	e)	What are the merits and demerits of TTL?	[4M]
	f)	Why sampling gates called linear gates and how do they differ from logic gates?	[4M]

PART -B

2	a)	An RC low-pass filter is fed with a symmetrical square wave. The peak-to-peak amplitude of the input waveform is 10 V and its average value is zero. It is given that RC=*T/2* where *T* is the period of the square wave. Determine the peak-to-peak amplitude of the output waveform.	[8M]
	b)	Draw the response of an RC high pass circuit when applied with exponential input. Explain the response for different time constants.	[8M]
3	a)	Draw the circuit diagram and explain the working of transistor clippers.	[6M]
	b)	Draw the basic circuit diagram of negative peak clamper circuit and explain its operation	[7M]
	c)	Give some applications of clipping & Clamping circuits.	[3M]
4	a)	Describe how a transistor functions as a switch in the CE configuration in ON state and in OFF state. How does the temperature affect the saturation junction voltages of a transistor?	[8M]
	b)	Classify the basic families that belong to the bipolar families and to the MOS families.	[4M]
	c)	What is the major difference between TTL and ECL? Why does the propagation delay occur in logic circuits?	[4M]

||''|'''|''|'|'|''''||

5 a) A self-biased binary uses n-p-n transistors have maximum values of V_{CE}(sat)=0.4V and V_{BE}(sat) = 0.8V and V_{BE} (cutoff) = 0V. The circuit parameters are V_{CC} = 15V, RC = 1KΩ, R1 = 6KΩ, R2 = 15KΩ and RE = 500Ω. i) Find the stable-state currents and voltages. ii) Find the minimum value of hFE required for BJT to provide the above stable state values. iii) Also determine I_{CBO}(max) to which I_{CBO} raises as temperature rises where neither BJT is off. [8M]

b) Explain various methods to improve the resolution of a binary. [4M]

c) Draw the circuit of a Schmitt trigger and give some of its applications. [4M]

6 a) Explain the basic principle of a bootstrap sweep generator. Draw the circuit and explain its operation. Derive the expression for its slope error. [8M]

b) How is deviation of linearity expressed? What do you mean by sweep time and restoration time? [8M]

7 a) What is meant by synchronization with frequency division? Explain, with suitable waveforms, the procedure to obtain 3:1 and 5:1 synchronization. [8M]

b) Draw the circuit diagram of a unidirectional sampling gate which delivers an output only at the coincidence of a number of control voltages and explain its working. [8M]

*****

||'|'''|'|'|''''||