Roll No. .....

MCA-11 (Master of Computer Applications)/ M.Sc.(IT)-12(Master of Science in Information Technology)/ PGDCA-11 (Post-Graduate Diploma in Computer Applications)

Second Semester Examination-2015

MCA-05/M.SC.(IT)-05/PGDCA-05

Computer Organization & Architecture

Time : 3 Hours **Maximum Marks :** 60

Note : This paper is of sixty (60) marks divided into three (03) sections A, B, and C. Attempt the questions contained in these sections according to the detailed instructions given therein.

Section - A

(Long Answer Type Questions)

Note : Section 'A' contains four (04) long-answer-type questions of fifteen (15) marks each. Learners are required to answer any two (02) questions only. (2×15=30)

1. Explain Wormhole routing for message-passing technique

2. (a) Write briefly about interrupt? How to handle multiple interrupts.

   (b) Discuss the Instruction Execution Cycle without interrupt and with interrupt

3. What do you mean by Addressing Mode? Discuss different types of addressing modes including the advantages and disadvantages of each mode.

4. Discus the basic concepts of pipelining. What is a pipeline hazard? What are the types of hazards?

Section - B

(Short Answer Type Questions)

Note : Section 'B' contains eight (08) short-answer-type questions of five (05) marks each. Learners are required to answer any four (04) questions only. (4×5=20)

1. What is the difference between parallel processing and pipeline processing?
2. Discuss about the Hardwired implementation of the Control Unit.
3. What is Bus? Draw the single bus structure.
4. What are the methods for determining which I/O device has requested an interrupt?
5. State and explain in brief Flynn's classification of Multiprocessor architecture.
6. Explain the concept of Virtual Memory.
7. What do you mean by locality of reference? What are its types?
8. Discuss memory disk caching with level 1 and level 2 cache.

Section - C

(Objective Type Questions)

Note : Section 'C' contains ten (10) objective-type questions of one (01) mark each. All the questions of this section are compulsory. (10×1=10)

1. In memory-mapped I/O

a) The I/O devices and the memory share the same address space

b) The I/O devices have a separate address space

c.) The memory and I/O devices have an associated address space

d) A part of the memory is specifically set aside for the I/O operation

2. In case of, Zero-address instruction method the operands are stored in ..... .

a) Registers b) Accumulators

c) Push down stack d) Cache

3. The method of access ing the I/O devices by repeatedly checking the status flags is

a) Program-controlled I/O b) Memory-mapped I/O

c) I/O mapped d) None

4. The bus connecting CPU, Memory and I/O is known as

a) Bus b) System Bus

c) Modem d) None of the above

5. The DMA differs from the interrupt mode by

a) The involvement of the processor for the operation

b) The method accessing the I/O devices

c) The amount of data transfer possible

d) Both a and c

6. The techniques which move the program blocks to or from the physical memory is called as ..... .

a) Paging

b) Virtual memory organisation

c) Overlays

d) Framing

7. ..... is communication path way between connecting two or more modes.

a) Bus b) System Bus

c) Modem d) None of the above

8. The technique where the controller is given complete access to main memory is

a) Cycle stealing b) Memory stealing

c) Memory Con d) Burst mode

9. The pipelining process is also called

a) Superscalar operation b) Assembly line operation

c) Von-neumann cycle d) None of the mentioned

10. The benefit of using hardwired control unit is

a) It is cost effective

b) It is highly efficient

c) It is very reliable

d) It increases the speed of operation