Code No: A5502, A5702 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, October/November 2011
VLSI TECHNOLOGY AND DESIGN
(COMMON TO EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Explain CMOS inverter voltage transfer characteristics with a neat diagram. What are the criteria for voltage threshold for high level and low level in inverter characteristics?
b) What is latch-up condition in CMOS circuits? How it can be eliminated. [12]

2.a) Determine the Pull-up to Pull-down ratio for an NMOS inverter driven through one or more pass transistors.
b) Explain about-NMOS logic, domino logic and DCVS logic and compare them. [12]

3.a) What are the varieties of design layout of wiring trees in the wires and delay?
b) With suitable diagrams explain some switch logic arrangements. [12]

4.a) Design the static complementary pull up and pull down networks for these expressions;
i) $\overline{(A+B+C)}$
ii) $\overline{[(A+B)C]}$
b) Draw a stick diagram for a three input NOR gate. [12]

5.a) Explain the standard cell layout design in combinational logic network.
b) Explain how the gate placement affects load capacitance in fanout of combinational logic. [12]

6.a) Explain the clocking Analysis related to sequential systems.
b) Draw and explain the cross section of a pair of stacked capacitor DRAM cell. [12]

7.a) Explain system-on-chip concept using platform based design.
b) What are the various floorplanning tips and explain it? [12]

8. Write a short note on
a) High level synthesis.
b) ASM chart design [12]

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