NR

Code No: A7004

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations, October/November-2011
VLSI ARCHITECTURE AND DESIGN METHODOLOGIES
(ELECTRONICS AND COMMUNICATION ENGINEERING)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

\- - -

1.a) Explain types of ASIC's.
b) Explain gate array based ASIC's and FPGA. [12]

2. Explain types of simulation in detail at system level. [12]

3.a) Explain the logic arrays.
b) Design a dynamic CMOS PLA based on NOR gate for the following functions.
$f_1 = (a.b.c+a'.b'.c')'$ $f_2 = (a.b.c)'$ [12]

4. Explain Xilinx XC 4000 Architecture with neat sketches. [12]

5. Explain ACT1 Architecture of FPGA with neat sketches. [12]

6. Explain cool runner –II Architecture of CPLD. [12]

7. Explain about low power design considerations. [12]

8. Explain in detail how VLSI Architecture influenced on modern robotics. [12]

* * * * * *