Code No: A7707 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M. Tech I Semester Examinations, October/November 2011
LOW POWER VLSI DESIGN
(EMBEDDED SYSTEMS AND VLSI DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Why Low power design is becoming the norm for all high-performance applications?
b) Explain the role of Interconnect wires in power consumption of an integrated circuit. [12]

2.a) Draw the Cross-sectional diagram of an npn bipolar transistor is added to a basic n-well CMOS process and explain how it processed?
b) How CDI structure achieves an isolation between adjacent bipolar devices? [12]

3.a) Explain the 0.6μm polysilicon emitter BiCMOS process flow with neat diagrams.
b) Write all electrical characteristics of SOI lateral BJT. [12]

4.a) What are the advantages of current model of Advanced MOSFET?
b) Draw the equivalent circuit of HICUM model of BJT and explain it. [12]

5.a) What are the three important model parameters that must be determined to develop the analytical model of sub-half micron MOS device?
b) How to determine the p+-implant junction depth for sub-half micron MOS devices? [12]

6.a) Draw the Basic Driver configuration and explain its working with V-I characteristics.
b) Compare the propagation delay versus capacitive load characteristics of various BiCMOS and CMOS circuits. [12]

7.a) How to eliminate the need of input protection circuits in the design of BiCMOS circuits?
b) Explain how ESD-free BiCMOS digital circuit maintains its speed performance leverage over the CMOS circuits? [12]

8. Write short notes on [12]
a) Evolution of Latches and Flip-Flops.
b) Power dissipation measures for Latches and Flip-Flops.

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