**NR**

**Code No: B5502, B6801, B5708**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**M.Tech II Semester Examinations, October/November 2011**

**DSP PROCESSORS AND ARCHITECTURES**

**(COMMON TO EMBEDDED SYSTEMS, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEMS DESIGN)**

**Time: 3hours** **Max. Marks: 60**

**Answer any five questions**

**All questions carry equal marks**

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1.a) In a DSP scheme show a continuous time signal, its sampled signal, sampled data signal Quantized digital signal & digital to analog converter output signal.

b) What is a system function? Explain how a LTI system is characterized. [12]

2. What is rounding error? Explain in context with ADC errors. Describe with an example ,DAC converter error due to the zero order. Differentiate between ADC and DAC errors in Computational accuracy in DSP. [12]

3.a) For a standard DSP FIR filter what are the basic features to investigate? Explain Organization of the On-Chip memory for DSProcesor.

b) Explain DSP Data addressing capabilities, with an example for each.

c) What are the special addressing modes in DSP? Give an example for each. [12]

4. Explain 3 stage pipelining and 5 stage pipelining, Justify your answer whether C54XX pipelining concept is employed. What is Perfect overlap in this situation seen in C54XX? What is pipeline hazard? With an example show reservation table for C54XX in pipelining. Explain Branching effects in pipelining. [12]

5. How will you configure a TMS320C5416 processor to have the following on chip memories? Specify the address range in: On chip ROM, for a program. How much RAM for data will be available in the specified configuration? [12]

6. Explain in detail PID controller in a continuous system. Explain the implementation of PID controller. [12]

7. Explain 4 point DFT computation with an example. [12]

8.a) Describe the memory interface block diagram of TMS320C5416.

b) Interface an 8Kx16 Program ROM to the C5416 in the address range 7FE000H-7FFFFFH.

c) Describe the I/O interface signals for READ-READ-WRITE sequence of operations. [12]

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