Code No: B0601 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II Semester Examinations, October/November 2011
DESIGN OF FAULT TOLERANT SYSTEMS
(DIGITAL SYSTEMS AND COMPUTER ELECTRONICS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Derive an expression for the term Reliability of a system which has a constant factor rate.
b) Show that the reliability of a parallel to series inter connection scheme of 4 modules A, B, C and D with identical reliability value is better than series to parallel inter connection scheme. [12]

2.a) Show that the MTBF of TMR system is less than that of a simple system. What is the methodology to improve MTBF of a TMR system?
b) Derive and explain the R (+) factor of a hybrid system with a TMR code and 3 spaces. [12]

3.a) Explain Reddy's realization of totally self clucking checker of 2 out of 5 codes.
b) Explain the procedure of designing a sub limit of check bit generator of a totally self checking checker for Bergu code. Use I = 15, k = 4. [12]

4.a) Discuss a synchronous sequential circuit for the given mealy machine below using partition theory to make it a fail safe design.

PS	NS, I_1	O/P I_2
S_0	$S_1, 0$	$S_0, 0$
S_1	$S_1, 0$	$S_2, 0$
S_2	$S_1, 0$	$S_3, 0$
S_3	$S_1, 1$	$S_0, 0$

b) Write a brief note on lowest residue code. [12]

5.a) Apply Reed Mullus expansion technique and realize the circuit along with test vector for the given function.
$f = A\overline{B} + \overline{B}C\overline{D} + C\overline{A}$
b) Briefly explain about syndrome testability and AND – OR – NOT realization of design for testable logic. [12]

6. List out the LSSD design rules and explain its advantages and disadvantages. Also explain the single catch design procedure. [12]

7.a) Write a brief note on weighted random pattern generator .
b) Explain the architecture of BILBO. [12]

8. Write a brief note on
a) Multi input signater register
b) Use of control logic with 5 test vectors to design for testability of combination logic. [12]

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