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Code No: B5503

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech II Semester Examinations, October/November 2011
CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(EMBEDDED SYSTEMS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks
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1.a) Give the functional description of the Altera's MAX 7000 PLD with the help of logical array block and Macro cell Diagrams.
b) Distinguish between the design and manufacturing steps of MPGA and FPGA and also explain the advantages of FPGA. [12]

2.a) Explain all the advanced features of the Xilinx 4000 Series FPGAS.
b) Explain about technology specific synthesis and the routing constraints with respect to XC4000. [12]

3.a) What is optimized reconfigurable cell array? Explain its architecture with neat diagrams.
b) Distinguish between the ACTEL'S PLDS with respect to architecture features, speed, area and power consumption. [12]

4.a) Explain how one hot encoding simplifies the next state calculation with the help of state machine diagrams and coding tables.
b) Develop one hot state diagram for a sequence checker whose output is '1' whenever the sequence 0101 is detected. Also specify the Transition Table. [12]

5.a) Explain about the traffic light controller as an example of pertinent with neat diagram and Sequence.
b) Explain about meta-stability with appropriate waveforms and suggest the methods of reducing meta stability. [12]

6.a) Explain the use of ASMS in one hot design
b) Explain about the state machine designs centered around shift registers. [12]

7.a) Explain about the FPGA Advantage Tool that allows different design entries.
b) Explain how you design an 8 bit counter using 8 D Flip Flops. [12]

8. Write short notes on any **TWO**
a) Lattice PLD architecture
b) Technology mapping for FPGAS
c) FSM system Level Design. [12]

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