Code No: C3803, C0601, C7003, C5503, C7703, C4507, C6803, C5703 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, March-2011

VLSI TECHNOLOGY AND DESIGN

(COMMON TO DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS, DIGITAL SYSTEM AND COMPUTER ELECTRONICS, ELECTRONICS & COMMUNICATION, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, SYSTEMS & SIGNAL PROCESSING, VLSI &EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1. a) What is latch-up condition in CMOS circuits? How it can be eliminated.
   b) What are the deficiencies of MOS technology? How do we over come them? [12]

2 a) explain the scalable design rules with equation
   b) Explain the pseudo-NMOS logic during the low to high transition. [12]

3 a) Explain the delay in combinational logic network and how combinational delay can be reduced.
   b) What are various switch logic circuits? Compare their merits and demerits. [12]

4. Explain about 1 -φ clocking rules for flip-flops and 2 -φ clocking disciplines for latches. [12]

5. a) What are various floor planning methods? Explain them clearly.
   b) With relevant diagrams explain about various Floor planning methods used in Layout design. [12]

6) a) Explain the technology independent and technology dependant strategies of logic optimization used in logic synthesis
   a) Explain briefly how the hardware/software Co-simulation and co- synthesis issued are addressed. [12]

7 a) Briefly explain the design validations in the floor planning.
   b) Describe the Placement and routing in floor planning. [12]

8.Write short notes of the following:
   a) power optimization.
   b) Inductive interconnect delays. [12]

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