R09

Code No: C0610, C8805

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.Tech I Semester Examinations March/April-2011
DIGITAL CONTROL SYSTEMS
(COMMON TO DIGITAL SYSTEMS & COMPUTER ELECTRONICS, ELECTRONICS & INSTRUMENTATION)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks

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1. Consider the system shown in Fig.P1, below. Derive the difference equation describing the system dynamics when the input voltage is pieceswise constant. i.e.,
   e(t) = e(kT) when kT ≤ t < (k + 1) and T = 1 Sec

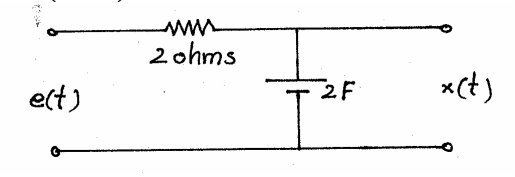


Fig.P1

Also obtain the values of the output voltage at sampling instants of e(kT) = kT for k ≥ 0. [12]

2. (a) Find the Z-transform of the following:
   (i) $f(t) = t^2$, (ii) $f(t) = e^{-\alpha t} \sin \omega t$
   (b) Find the inverse Z-Transform of the following
   (i) $F(z) = \dfrac{z-4}{(z-1)(z-2)^2}$, (ii) $F(z) = \dfrac{3z^2+2z+1}{(z^2-3z+2)}$.

3. The pulse transfer function of digital control systems is given by

$$G(z) = \frac{5z}{z^2+2z+2}$$

Obtain a state space representation for the system and draw the state diagram. Also obtain the state transition matrix. [12]

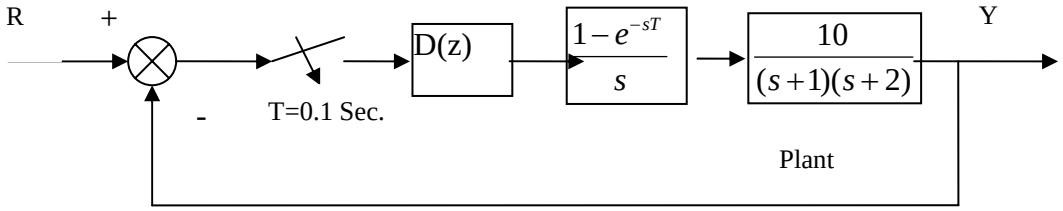
4. (a) Derive the necessary condition for the digital control system
   X(k + 1) = AX(k) + Bu(k)
   C(k) = DX (k) to be controllable.
   (b) Investigate the controllability and observability of the digital system.

$$X(k+1) = \begin{bmatrix} -1 & 1 \\ 0 & -1 \end{bmatrix} X(k) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u(k) \text{ and } \quad y(k) = [1 \quad 1]\, X(k)$$ [12]

5. (a) Explain the pole-placement technique for design of digital controller.
   (b) Consider the single input digital control system
   X(k + 1) = AX(k) + Bu(k)
   where $A = \begin{bmatrix} 0 & 1 \\ -2 & -3 \end{bmatrix}$, $B = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$
   Determine, the state feed back matrix K such that the state feed back u(k) =-KX(k), places the closed loop system poles at 0.3 ±j0.3.

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6. A block diagram of a digital control system is shown below. Design a PID controller D(z), to eliminate the steady-state error due to a step input and simultaneously realizing a good transient response, and the ramp-error constant K_v should equal 5.



7. (a) Explain the design procedure of digital control through bilinear transformation method.
(b)Explain a method based on state space to find the response between two consecutive sampling instants. [12]

8. (a) With a neat schematic diagram, explain the design reduced order observer.
(b) Consider the digital process with the state equations described by

$X(k+1) = AX(k) + Bu(k)$
$y(k) = C\,X(k)$

where $A = \begin{bmatrix} 0 & 1 \\ -1 & 1 \end{bmatrix}$, $B = \begin{bmatrix} 0 \\ 1 \end{bmatrix}$, $C = \begin{bmatrix} 2 & 0 \end{bmatrix}$.

Design a full order observer which will observe the states $x_1(k)$ and $x_2(k)$ from the output c(k), having dead beat response. [12]

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