Code No:D5502 **R09**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II SEMESTER EXAMINATIONS, APRIL/MAY 2012
DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES
(EMBEDDED SYSTEMS)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks
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1.a) Prove that filters with symmetrical impulse response have linear phase.
b) Explain different sources of noise and their corresponding effects considering finite word length effects in FIR filter.

2.a) Design a digital filter equivalent of a 2nd order Butterworth low-pass filter with a cut-off frequency f_c = 100 Hz and a sampling frequency f_s = 1000 samples/sec. Derive the finite difference equation and draw the realization structure of the filter. Given that the analogue prototype of the frequency-domain transfer function $H(s)$ for a Butterworth filter is: $H(s) = \frac{1}{S^2 + \sqrt{2}S + 1}$
b) Calculate the number of bits required to produce a SNR of 30dB for a sine wave acquisition that varies between 0.5V to 6V.

3.a) Explain basic features common to virtually all DSP processors and explain the use of each feature.
b) Explain about floating point emulation and block floating-point.

4.a) Explain about the following DSP computational building blocks with neat diagrams
i) Barrel shifter
ii) MAC unit
iii) ALU unit
b) Explain the bit reversed and circular addressing modes with suitable examples.

5.a) Explain about the FIRS instruction of TMS320C54XX with an example.
b) What is pipelining? Explain how pipelining is useful for reducing the number of instruction cycles with examples.

6.a) If decimation by a factor of 8 is achieved by decimating by a factor of 2 followed by another factor of 4, determine the cutoff frequencies of the two low pass filters that should be used in the decimation.
b) Write a TMS320C54XX program for the PID controller.

7.a) Explain the interfacing of PCM3002 codec with TMS320VC5416 DSK using block diagram and transmission formats.

b) Explain the implementation of 8-point FFT on the TMS320C54XX with an assembly code.

8.a) Explain the addressing technique used for configuring the DMA registers of a DSP Processor.

b) Write a TMS320C54xx code to transfer a block of data from the program memory to the data memory. Following are the specifications Source address:
5000h in program space;
Destination address: 7000h in data space;
Transfer size: 600h single (16-bit) words;
Channel used: DMA channel #1.

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