R09

Code No: D4305

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012
DIGITAL CONTROL SYSTEMS
(POWER ELECTRONICS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) State and prove the sampling theorem.

b) Given the error function as $E(s) = \frac{10(s+2)}{s^2(s^2+2s+2)}$. Based upon the sampling theorem, determine the maximum value of the sampling interval T that can be used to enable to reconstruct e(t) from its samples.

2.a) Obtain the z-transform following:

(i) $X(s) = \frac{1}{s^2(s+1)}$ and

(ii) $f(t) = e^{-\alpha t} t^2$.

b) Determine y(∞) for the following Y(z) function ('**a**' is a real constant):

$$Y(z) = \frac{K[z^3 - 2az^2 + (a^3 - a^2 + a)z]}{(z-1)(z-a)(z-a^2)}$$

Assuming stable response, determine what the value of K must be for y (∞) =1.

3. The pulse transfer function of digital control systems is given by

$$G(z) = \frac{5z}{z^2 + 2z + 2}$$

Obtain a state space representation for the system and draw the state diagram. Also obtain the state transition matrix.

4.a) Derive the necessary condition for the digital control system
X(k + 1) = AX(k) + Bu(k)
Y(k) = CX (k)
to be Controllable.

b) Examine whether the discrete data system

$$X(k+1) = \begin{bmatrix} 1 & -2 \\ 1 & -1 \end{bmatrix} X(k) + \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix} U(k) \text{ and } Y(k) = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} X(k)$$ is

(i) State controllable,
(ii) Output controllable and
(iii) Observable.

5.a) The block diagram representation of digital control system is shown in Fig. P5

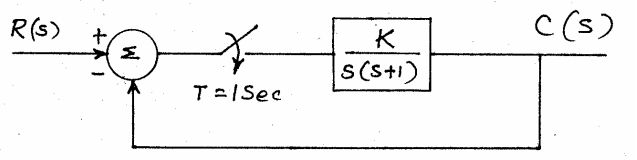


Fig. P5

Using Jury's criterion, find the range of values of K for which the system is stable.

b) Explain the Lyapunov's stability theorem for linear digital control system.

6.a) Explain the deadbeat response characteristics. The plant transfer function of a digital control system shown below Fig P6 is given by $G_p(z) = \dfrac{z^{-2}}{1 - z^{-1} - z^{-2}}$, design a digital controller so that a dead beat performance is obtained when the input is a unit step function.

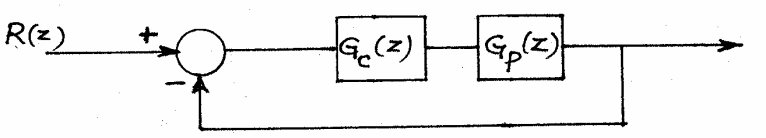


Fig. P6

b) Explain the design procedure of digital controller through bilinear transformation.

7.a) With a neat schematic diagram, explain the design procedure of full order observer.

b) Consider the digital process with the state equations described by

$$X(k+1) = \begin{bmatrix} 0 & 1 \\ -1 & 1 \end{bmatrix} X(k) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} u(k) \quad \text{and} \quad y(k) = \begin{bmatrix} 2 & 0 \end{bmatrix} X(k)$$

Design a first order observer which will observe the state $x_2(k)$ from the output c(k), having dead beat response.

8.a) Consider the multi-input digital control system

$$X(k+1) = \begin{bmatrix} 0 & 1 \\ -1 & -2 \end{bmatrix} X(k) + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} U(k)$$

Determine the feedback matrix K such that the state feedback u(k) = -KX(k) places the closed loop poles at $z_1 = 0.1$ and $z_2 = 0.2$.

b) Explain the Kalman filter algorithm for state estimation of dynamical systems with clearly indicating its assumptions.

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