R09

Code No: D5504

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012
CPLD AND FPGA ARCHITECTURE AND APPLICATIONS
(EMBEDDED SYSTEMS)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1.a) Explain about Cypress Flash device technology and also explain about the merits and demerits of the technology.
b) Explain about AMD's CPLD features and different categories of the same.

2.a) Explain about the FLEX and FLEX8000 logic array block architecture with neat diagrams.
b) Compare the following FLEX8000 family with respect to logic elements, Flip Flops and usable gates.
(i) EPF8686 (ii) EPF8820 (iii) EPF81188 (iv) EPF81500

3.a) Explain the basic concepts and properties of petrinets for state machine.
b) Give the description of a traffic light controller using the petrinet.

4.a) Draw and explain different design stages involved in the FPGA design flow
b) Compare the different family members of XC4000 with respect to the CLB array size, Input Outputs and gate capacity.

5.a) Explain how multiplexer based approach is useful for the design of an ALU
b) Explain the operation of a small petrinet controller.

6.a) Explain the use of ASMS in one hot design
b) Explain about the state machine designs centered around shift registers.

7.a) Explain about the FPGA Advantage Tool that allows different design entries.
b) Explain how you design an 8 bit counter using 8 D Flip Flops.

8. Write short notes on any TWO
a) Lattice PLD architecture
b) Technology mapping for FPGAS
c) FSM system Level Design

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