Code No: B5508, B5702 **NR**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH II SEMESTER EXAMINATIONS, APRIL/MAY 2012
DESIGN FOR TESTABILITY
(COMMON TO EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions
All questions carry equal marks

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1. Define the following fault models using examples:
   a) Bridging fault
   b) path-delay fault
   c) Cross-point fault.

2. a) How the effect of a fault is represented by means of a model? Explain the single stuck-at fault model with example.
   b) Explain what action an event-driven true-value simulator will take when it evaluates a zero-delay gate.

3. a) Write a procedure for completely fault-locatable networks for unite functions.
   b) Explain Triple Modular Redundancy masking technique for faulty components in circuit.

4. a) How the path sensitization method is used to generate a test pattern for combinational circuits?
   b) Prove that if a combinational test vector can be obtained for a fault in the pseudo-combinational circuit, then that vector repeated as many times as *sequential depth +1* will always detect the corresponding fault in the sequential circuit.

5. a) What are the properties of a testable circuit?
   b) How the control logic can be used to increase the observability and controllability?

6. a) Explain the test procedure for syndrome-testable circuit with suitable block diagram.
   b) Draw a modulo-3 circuit diagram illustrating scan design and test generation and also explain its working.

7. a) Explain why BIST is the preferred form of DFT?
   b) Draw the block diagram for a BIST implementation using BILBO and explain the test procedure.
   c) What is STUMPS? Explain how it is used for test-per-scan testing system?

8. a) How mutual comparator is useful in memory BIST when the memory system has multiple arrays?
   b) Explain the counter test technique for RAM BIST.

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