Code No: RR220501 **Set No. 1**

II B.Tech II Semester Supplimentary Examinations, Apr/May 2008
COMPUTER ORGANIZATION
(Common to Computer Science & Engineering, Information Technology, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about IAS memory formats.
   (b) List various registers in a computer along with their purpose [8+8]
2. (a) Find the output binary number after performing the following arithmetic operations
      i. 111.01 + 10.111
      ii. 11.01 + 110.11
      iii. 110.11 - 111.01
   (b) Explain about the longhand division of binary integers. [6+10]
3. (a) Describe various Pentium data types
   (b) Describe various common data transfer instruction set operations. [6+10]
4. (a) List various R3000 pipeline stages. Also explain the function of each.
   (b) List and describe all shift and multiply/divide instructions of MIPS R-Series processors. [8+8]
5. (a) Differentiate between single versus two-level caches.
   (b) Elaborate on Pentium Cache Organization. [8+8]
6. Discuss three possible techniques for I/O operations with merits and demerits of each. [16]
7. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer [6+6+4]
8. (a) Give a summary of arithmetic and logical operations that are defined for the vector architecture.
   (b) What is cache coherence problem. Discuss about different cache coherance approches. [8+8]

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Code No: RR220501 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the purpose and merits of interrupts.
   (b) Draw and explain the instruction cycle with interrupts.
   (c) What is interrupt handler? Explain its purpose. [6+6+4]
2. (a) How subtraction is done on the binary numbers represented in one's complement notation give an examples.
   (b) What do you mean by r's complement. [8+8]
3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. [16]
4. Elaborate on different types of registers in a register organization [16]
5. Discuss about address translation with segmentation and paging in the Intel Pentium [16]
6. (a) How would CPU handles multiple devices. Explain with different techniques available
   (b) Discuss the characteristics of Intel 8259A interrupt controller. [8+8]
7. (a) Discuss about I/O channel architecture.
   (b) Discuss about I/O addressing in 8086.
   (c) Discuss the salient features of laser printer [6+6+4]
8. (a) Classify and explain different multiprocessors
   (b) Explain the organization of tightly coupled multiprocessor system with a generic block diagram. [8+8]

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Code No: RR220501 **Set No. 3**

II B.Tech II Semester Supplimentary Examinations, Apr/May 2008
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Define PCI. Explain the applications of PCI
   (b) Describe any ten mandatory PCI signals. [8+8]
2. Write an algorithm to substract binary numbers represented in normalized floating point mode with base 2 for exponent [16]
3. NOOP instruction has no effect on the CPU state other than incrementing the program counter. Suggest some uses of this instruction with examples. [16]
4. Elaborate on different types of registers in a register organization [16]
5. Give a block diagram for a 4M×8 memory using 256K×1 memory chips. [16]
6. (a) Explain about magnetic disk layout
   (b) Elaborate on Winchester disk track format. [8+8]
7. (a) Explain about microinstruction format of TI 8800
   (b) Explain about ALU control fields of IBM 3033 microinstruction. [8+8]
8. (a) Explain the following terms.
      i. Read miss
      ii. Read hit
      iii. Write miss
      iv. Write hit
   (b) Discuss different approaches to vector computation [8+8]

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Code No: RR220501 **Set No. 4**

II B.Tech II Semester Supplimentary Examinations, Apr/May 2008
COMPUTER ORGANIZATION
(Common to Computer Science & Engineering, Information Technology, Computer Science & Systems Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss the interconnection structure design of a computer.
   (b) Explain various bus lines.
   (c) What do you mean by multiple - bus hierarchies. [8+4+4]
2. (a) Find the output binary number after performing the arithmatic operation using 1's complement representation.
      i. 111.01 + 10.111
      ii. 110.11 - 111.01
   (b) Explain steps involved in the addition of numbers using 2's complement notation. [10+6]
3. Discuss about various Pentium addressing modes with algorithms [16]
4. (a) List various R3000 pipeline stages. Also explain the function of each.
   (b) List and describe all shift and multiply/divide instructions of MIPS R-Series processors. [8+8]
5. (a) Discuss about address translation in paging.
   (b) How does page size effects storage utilization and effective memory data-transfer rate [8+8]
6. Discuss about data organization and formatting of magnetic disk in detail [16]
7. Discuss about horizontal and vertical instruction formats. Also differentiate between horizontal and vertical instruction formats. [16]
8. (a) Explain different types of parallel processors.
   (b) What do you mean by compound instruction? Give examples
   (c) Elaborate on registers of the IBM3090 vector facility. [4+6+6]

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