Code No: R05310402 **Set No. 1**

III B.Tech I Semester Regular Examinations, November 2008
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Design a 4-input CMOS OR-AND-INVERT gate. Explain the circuit with the help of logic diagram and function table?
   (b) Explain the following terms with reference to CMOS logic.
      i. Logic '0' and Logic '1'
      ii. Noise margin
      iii. Power supply rails
      iv. Propagation delay [10+6]

2. (a) Draw the circuit diagram of basic CMOS gate and explain the operation.
   (b) List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74LS00. [8+8]

3. (a) Write a VHDL Entity and Architecture for the following function.

$$F(x) = (a + b)(c \oplus d)$$

   Also draw the relevant logic diagram.
   (b) Write a VHDL Entity and Architecture for a 3-bit ripple counter using Flip-Flops? [8+8]

4. (a) Write a VHDL program in Behavioral style to generate a clock with off time and on time equal to 10ns.
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function. [8+8]

$$F(P) = \Pi_{A,B,C,D}(1, 7, 9, 13, 15)$$

5. (a) Draw the logic symbol of 74X245 and explain its operation?
   (b) Write a VHDL program for 74X245? [16]

6. (a) Design a barrel shifter for 8-bit using three control inputs. Write a VHDL program for the same in data flow style.
   (b) Design a priority encoder with 8 inputs. Write a VHDL program for the same in structural style. [8+8]

7. (a) Design a conversion circuit to convert a D flip-flop to J-K flip-flop. Write data-flow style VHDL program.

(b) Design a 4-bit binary synchronous counter using 74X74? Write VHDL program for this logic using data flow style. [8+8]

8. (a) How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and twos complement overflow output? Show the block schematic with all inputs and outputs?

(b) Design an 8×4 diode ROM using 74X138 for the following data starting from the first location. [8+8]

$$B, 2, 4, F, A, D, F, E$$

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Code No: R05310402 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.
   (b) Design a CMOS transistor circuit for the following functional behavior.

$$f(x) = \overline{(\mathrm{b} + \mathrm{c})(\mathrm{a} + \overline{\mathrm{c}})}$$

   Also draw the relevant circuit diagram. [8+8]

2. (a) Compare CMOS, TTL and ECL with reference to logic levels, DC Noise margin, propagation delay and fan-out.
   (b) List out different categories of characteristics in a TTL data sheet? Discuss electrical and switching characteristics of 74LS00. [6+10]

3. (a) Explain the various data types supported by VHDL. Give the necessary examples.
   (b) Explain with an example the syntax and the function of the following VHDL statements?
      i. Loop statement
      ii. Case statement [8+8]

4. (a) Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.
   (b) Explain data-flow design elements of VHDL. [10+6]

5. (a) Using two 74×138 decoders design a 4 to 16 decoder?
   (b) Write a data flow style VHDL program for the above design? [10+6]

6. (a) Design a barrel shifter for 8-bit using three control inputs. Write a VHDL program for the same in data-flow style.
   (b) Write a VHDL program for the circuit that counts number of Zeros in a 16-bit register. Using structural style of modeling. [8+8]

7. (a) Design a switch debouncer circuit using 74X109 IC. Explain the operation using timing diagram.
   (b) Discuss the logic circuit of 74X377 register. Write a VHDL program for the same in structural style. [8+8]

8. (a) Explain how a 4×4 binary multiplier can be designed using 256x8 ROM.
   (b) Realize the logic function performed by 74×381 with ROM. [8+8]

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Code No: R05310402 **Set No. 3**

III B.Tech I Semester Regular Examinations, November 2008
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.
   (b) Analyze the fall time of CMOS inverter output with $R_L = 100\Omega, V_L = 2.5V$ *and* $C_L = 10PF$. Assume V_L as stable state voltage. [8+8]
2. (a) Draw the circuit diagram of basic CMOS gate and explain its operation
   (b) What are the typical parts of a TTL data sheet and discuss their importance in circuit design? [8+8]
3. (a) Discuss the steps in VHDL design flow.
   (b) What are the different data objects supported by VHDL? Explain scalar types with suitable examples. [8+8]
4. Design the logic circuit and write a data-flow style VHDL program for the following functions.
   (a) $F(X) = \Pi_{A,B,C,D}\,(1, 7, 9, 13, 15)$
   (b) $F(Y) = \Sigma_{A,B,C,D}\,(1, 4, 5, 7, 12, 14, 15) + d\,(3, 11)$ [8+8]
5. (a) Design a full adder using two half adders. Write VHDL data flow program for the same.
   (b) Design a 4×4 combinational multiplexer and write the corresponding VHDL program. [8+8]
6. (a) Write a VHDL program for an 8-bit comparator circuit using structural style of modeling.
   (b) Design a 16-bit comparator using 74X85 ICs. Draw the relevant circuit diagram. [8+8]
7. (a) Draw the logic diagram of 74X174 IC and explain the operation. Develop the VHDL model for this IC.
   (b) Design a switch debouncer circuit using 74X109 IC Explain the operation using timing diagram. [16]
8. (a) Design an 8x4 diode ROM using 74X138 for the following data starting from the first location.

$$1, 4, 9, B, A, 0, F, C$$

(b) Draw the internal structure of synchronous SRAM and explain its operation? [8+8]

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Code No: R05310402 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Design CMOS transistor circuit for 2-input AND gate. Explain the circuit with the help of function table?
   (b) Draw the resistive model of a CMOS inverter circuit and explain its behavior for LOW and HIGH outputs. [8+8]
2. (a) Draw the circuit diagram of two-input 10K ECL OR gate and explain its operation.
   (b) List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74LS00. [8+8]
3. (a) Explain with an example the syntax and the function of the following VHDL statements:
      i. Process Statement
      ii. Case Statement
   (b) Explain Implicit and Explicit visibility of a Library in VHDL? [8+8]
4. Design the logic circuit and write a data-flow style VHDL program for the following functions.
   (a) $F(X) = \Sigma_{A,B,C,D}\,(0, 2, 5, 7, 8, 10, 13, 15) + d\,(1, 6, 11)$
   (b) $F(Y) = \Pi_{A,B,C,D}\,(1, 4, 5, 7, 9, 11, 12, 13, 15))$ [8+8]
5. (a) Design a priority encoder for 16 inputs using two 74X148 encoders?
   (b) Write a behavioral VHDL program for the above design? [16]
6. A simple floating-point encoder converts 16-bit fixed-point data using four high order bits beginning with MSB. Design the logic circuit and write VHDL data-flow program. [16]
7. (a) Design an 8-bit serial-in and parallel-out shift register with flip-flops. Explain the operation with the help of timing waveforms.
   (b) Write VHDL data-flow program for the above shift-register. [8+8]
8. (a) Discuss how PROM, EPROM and EEPROM technologies differ from each other.
   (b) With the help of timing waveforms, explain read and write operations of SRAM. [8+8]

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