Code No: R05221901 **Set No. 1**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2008
COMPUTER ORGANISATION
(Common to Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
   (b) Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.
   (c) Distinguish between tightly coupled microprocessors and tightly coupled Microprocessors. [16]
2. Design a circuit to increment, decrement, complement and clear a 4 bit register using RS flip-flops. Explain the control logic. [16]
3. (a) Give the typical horizontal and vertical microinstruction formats. [8]
   (b) Describe how microinstructions are arranged in control memory and how they are interpreted. [8]
4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
5. Explain the following Cache Mapping Techniques
   (a) Direct Mapping
   (b) Set Associative Mapping. [8+8]
6. Explain the following:
   (a) Asynchronous Serial Transfer
   (b) Asynchronous Communication Interface. [8+8]
7. Explain the following with related to the Instruction Pipeline
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding

(e) Delayed load

(f) Pre-fetch target instruction

(g) Branch target buffer

(h) Delayed branch. [8×2=16]

8. (a) Explain the working of 8 x 8 Omega Switching network.

(b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]

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Code No: R05221901 **Set No. 2**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2008
COMPUTER ORGANISATION
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about various buses such as internal, external, backplane, I/O, system, address, data, synchronous and asynchronous.
   (b) Explain about daisy chain based bus arbitration. [16]
2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops. [8]
   (b) What are register transfer logic languages? Explain few RTL statement for branching with their actual functioning. [8]
3. (a) Why do we need subroutine register in a control unit? Explain. [8]
   (b) Explain nanoinstructions and nanometry. Why do we them? [8]
4. (a) Explain Booth's algorithm with its theoretical basis. [8]
   (b) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8]
5. Compare and contrast Asynchronous DRAM and Synchronous DRAM. [16]
6. What are the different modes of data transfer? Explain each mode in detail. [16]
7. (a) What is meant by instruction pipeline? Explain four segment Instruction Pipeline.
   (b) Give the timing diagram of instruction pipeline. [8+8]
8. (a) Explain multiport memory organization with a neat sketch.
   (b) Explain system bus structure for multiprocessors with a neat sketch. [8+8]

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Code No: R05221901 **Set No. 3**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2008
COMPUTER ORGANISATION
(Common to Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain about sign magnitude and 2's complement approaches for representing the fixed point numbers. Why 2's complement is preferable.
   (b) Give means to identify whether or not an overflow has occurred in 2s complement addition or subtraction operations. Take one example for each possible situation and explain. Assume 4 bit registers.
   (c) Distinguish between tightly coupled microprocessors and tightly coupled Microprocessors. [16]

2. Design register selection circuit to select one of the four 4-bit registers content on to bus. Give fuller explanation. [16]

3. (a) Differentiate between microprogramming and nanoprogramming. [8]
   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [8]

4. (a) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications. [8]
   (b) Explain single precision and double precision calculations. In general how many bytes are used for both and what is the precision we get. Give some examples where double precision calculations are needed. [8]

5. (a) Explain how the Bit Cells are organized in a Memory Chip. [8]
   (b) Explain the organization of a 1K x 1 Memory with a neat sketch. [8]

6. (a) Explain programmed I/O in detail.
   (b) Explain interrupt initiated I/O in detail. [8+8]

7. Explain the following with related to the Instruction Pipeline
   (a) Pipeline conflicts
   (b) Data dependency
   (c) Hardware interlocks
   (d) Operand forwarding
   (e) Delayed load
   (f) Pre-fetch target instruction

(g) Branch target buffer

(h) Delayed branch. [8×2=16]

8. (a) Explain the working of 8 x 8 Omega Switching network.

(b) Explain the functioning of Binary Tree network with 2 x 2 Switches. Show a neat sketch. [8+8]

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Code No: R05221901 **Set No. 4**

II B.Tech II Semester Supplimentary Examinations, Aug/Sep 2008
COMPUTER ORGANISATION
(Common to Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss about Flynn's classification of computers.
   (b) Explain about communication topologies used in multiprocessors. [16]
2. (a) What is the use of buffers. Explain about tri-state buffers. Explain about high impedance state. [6]
   (b) Explain commonly employed bit shift operators such as shift left, right, circular shift left/right and arithmetic shift left/right. Assume an 8-bit register, give an example for each [10]
3. (a) Why do we need subroutine register in a control unit? Explain. [8]
   (b) Why do we need some bits of current microinstruction to generate address of the next microinstruction? Support with a live example. [8]
4. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove. [8]
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [8]
5. (a) What is Redundant Array of Inexpensive Discs? What are the advantages of using this kind of systems?
   (b) Explain different levels of RAID. [8+8]
6. (a) What is Direct Memory Access? Explain the working of DMA.
   (b) What are the different kinds of DMA transfers? Explain.
   (c) What are the advantages of using DMA transfers? [8+4+4]
7. Write short notes on the following:
   (a) Arithmetic pipeline
   (b) Four segment instruction pipeline
   (c) Timing diagram of instruction pipeline. [5+5+6]
8. (a) Explain srial abitration (Daisy Chain).
   (b) Explain prallel abitration. [8+8]

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