Code No: R05210404 **Set No. 1**

II B.Tech I Semester Supplimentary Examinations, November 2008
ELECTRONIC CIRCUIT ANALYSIS
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Give the typical values for h-parameters of CC configuration. In general, for any transistor configuration prove that $Y_0 = h_0 \left(\frac{R_S + R_{i\infty}}{R_S + R_{i0}}\right)$ where $R_{i\infty} \equiv R_i$ for $R_L = \infty$ and $R_{i0} \equiv R_i$ for $R_L = 0$.
   (b) For CE amplifier , what is the maximum value of R_S for which R_o differs by no more than 10 percent of its value for RS = 0. The h-parameter values are $h_fe = 50, h_ie = 1.1K\Omega, h_{re} = 2.5x10^{-4}, h_{oe} = 25\mu A/V$. (10+6)

2. (a) Explain the significance of Miller's theorem in transistor circuit analysis.
   (b) Draw the circuit diagram of Difference amplifier and explain its operation.
   (c) Write a short note on Gain-Bandwidth product of amplifiers. [6+5+5]

3. (a) Draw Hybrid - π model for a transistor in the CE configuration and explain the significance of every component in this model.
   (b) Given a germanium p-n-p transistor whose basewidth is 10^{-4} cm. At room temperature and for a dc emitter current of 2 mA, find
      i. emitter diffusion capacitance,
      ii. f_T [Assume Diffusion constant as 47 cm^2/sec]. [8+8]

4. (a) What is Harmonic distortion in transistor amplifier circuits? Discuss second harmonic distortion. [8]
   (b) Draw and explain the operation of Class-AB power amplifier. How will it eliminate cross over distortion. [8]

5. (a) Draw and explain the circuit diagram of a single tuned Capacitance coupled amplifier. Also explain its operation?
   (b) Draw and explain the significance of Gain versus Frequency curve of tuned amplifiers when they are used in radio amplifiers?
   (c) Draw the Ideal and actual frequency response curves of a single tuned amplifier? [8+4+4]

6. (a) What is synchronous tuning ? Derive an expression for bandwidth of an n-stage synchronously tuned amplifier?
   (b) Show that for an 'n' stage synchronously tuned amplifier, maximum. bandwidth is obtained when the single stage gain is 4.34dB. [8+8]

7. (a) With the help of a neat circuit diagram, explain the operation of BJT shunt voltage regulator.
   (b) What is a voltage reference? Why is it needed?
   (c) What is the function of a series pass transistor? [8+4+4]

8. (a) Specify suitable component values to get Vo=7.5V in the circuit of (Given figure8a). Using a 7805 regulator. From data sheet. I_Q=4.2mA and V_R=5V, choose I_{R1}=25mA.

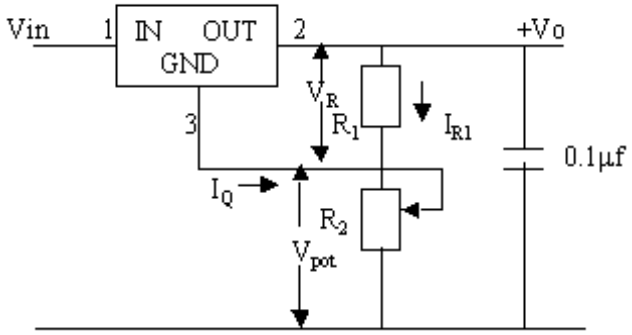

Figure 8a

   (b) Draw the functional diagram SMPS and explain its operation.

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Code No: R05210404 **Set No. 2**

II B.Tech I Semester Supplimentary Examinations, November 2008
ELECTRONIC CIRCUIT ANALYSIS
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the circuit diagram of Common Drain amplifier and derive an expression for its Voltage gain.
   (b) The h-parameters of the transistor used in CE amplifier are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10^{-4}, h_{oe} = 24μ A/V. Find out current gain and voltage gains with and without source resistance, input and output impedances, given that R_L= 10K and R_S= 1 K. [6+10]

2. (a) Explain the significance of Miller's theorem in transistor circuit analysis.
   (b) Draw the circuit diagram of Difference amplifier and explain its operation.
   (c) Write a short note on Gain-Bandwidth product of amplifiers. [6+5+5]

3. (a) Draw the small signal equivalent circuit for an emitter follower stage at high frequencies.
   (b) Consider a CE stage with a resistive load R_L. Using Miller's theorem Find out input capacitance at mid-band frequencies and high frequencies? [8+8]

4. (a) In series fed Class - A power amplifier, explain the importance of the position of operating point on output signal swing. Show that the conversion efficiency is 25%.
   (b) Discuss the origin of various distortions in transistor amplifier circuits. [10+6]

5. For the circuit shown in figure 5:
   (a) Draw the small signal equivalent circuit.
   (b) Derive Voltage gain (A_V).
   (c) Derive the expression for resonant frequency.
   (d) Voltage gain at resonant frequency (A_{res}).
   (e) Quality factor of the resonant circuit. [16]

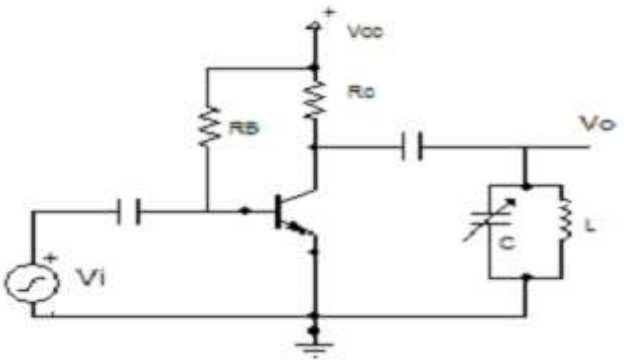

Figure 5

6. (a) Draw the Gain versus Frequency response of uncompensated and high frequency compensated CE wide band amplifier assuming that the lower 3-dB frequency is zero.

   (b) Explain High frequency compensation and what are the methods provided to achieve High frequency compensation in a CE amplifier? [8+8]

7. (a) The voltage regulator in Figure 7a maintains an output voltage of 25 V.

   i. What value of Rsc should be used to limit the maximum current to 0.5A?

   ii. With the value of Rsc found in (i) what will be the output voltage when RL= 100 ohms? When RL =10 ohms?

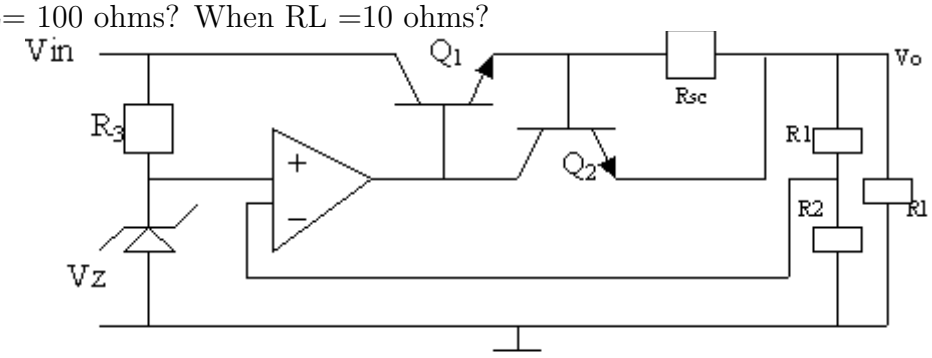

Figure 7a

   (b) Draw and explain the regulator which will provide the foldback limiting .[8+8]

8. (a) Explain the significance of Low Pass Filter in Switching Regulator

   (b) What are the limitations of Switching Regulators?

   (c) Why switching frequencies are limited in Switching regulator and also explain how to overcome this. [6+4+6]

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Code No: R05210404 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) For a single stage transistor amplifier, R_S=10K and R_L= 10K. The h-parameter values are h_{fc}= - 51, h_{ic} =1.1KΩ, h_{rc} ≈1, h_{oc} = 25 μA/V. Find A_I, A_V, A_{VS}, R_i, and R_o for the CC transistor configuration.
   (b) For a single stage transistor amplifier, R_S=5K and R_L= 10K The h-parameter values are h_{fe} = 50, h_{ie} =1.1KΩ, h_{re} = 2.5x10^{-4}, h_{oe} = 25 μA/V. Find A_I, A_V, A_{VS}, R_i, and R_o for the CE transistor configuration. [8+8]

2. (a) Draw the circuit diagram of Difference amplifier and explain its operation.
   (b) For the Cascode transistor configuration, which consists of CE stage in series with CB stage , verify that the cascode combination acts like a single CE transistor with negligible internal feedback. [8+8]

3. Derive all components in the Hybrid - π model in terms of h parameters in CE configuration. [16]

4. (a) With the help of a circuit diagram, explain the principle of operation of a class-C power amplifier.
   (b) What is the necessity of Heatsinks for a power transistor?
   (c) For a linear duration of power dissipation of a transistor with θ_{JC} (Junction-to-case) of 3.12% C/Watts and θ_{CS} (Case-to-heatsink) of 0.5^0C/Watt and θ_{SA} $(Heatsink - to - Ambient) of 4^0 C/Watts$, Obtain the maximum power dissipated by the transistor at 50^0C for a maximum junction temperature specification of 150^0C.

   [6+5+5]

5. For the circuit shown in figure 5:
   (a) Draw the small signal equivalent circuit.
   (b) Derive Voltage gain (A_V).
   (c) Derive the expression for resonant frequency.
   (d) Voltage gain at resonant frequency (A_{res}).
   (e) Quality factor of the resonant circuit. [16]

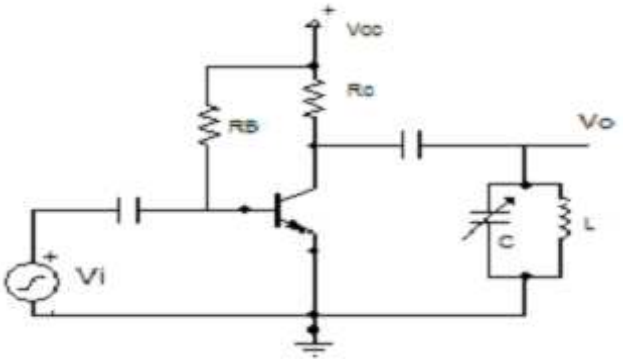

Figure 5

6. Explain what you mean by Synchronous tuning of tuned amplifiers? Draw the frequency response of a synchronously tuned amplifier showing the response of individual stages and overall responses? [16]

7. (a) What type of protection circuits are required in power supplies?
   (b) A 50V power supply has line regulation 0.2%V. How large would the 75V input voltage to the supply have to become for the output voltage to rise to 52V?
   (c) Give the disadvantages of the series and shunt regulators. [4+6+6]

8. (a) Specify suitable component values to get Vo=7.5V in the circuit of (Given figure8a). Using a 7805 regulator. From data sheet. I_Q=4.2mA and V_R=5V, choose I_{R1}=25mA.

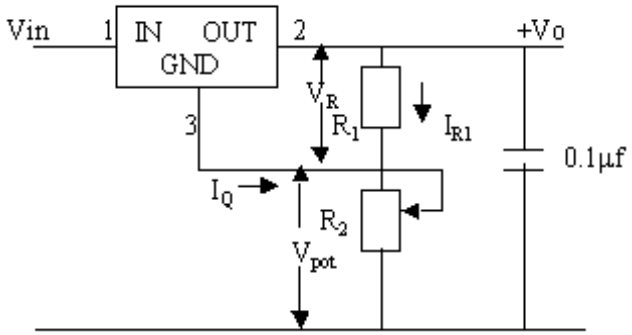

Figure 8a

   (b) Draw the functional diagram SMPS and explain its operation.

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Code No: R05210404 **Set No. 4**

II B.Tech I Semester Supplimentary Examinations, November 2008
ELECTRONIC CIRCUIT ANALYSIS
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Derive the expressions for A_i, A_V of CE amplifier circuit. Explain how A_i and A_V are effected by R_L.
   (b) Consider a single stage CE amplifier with R_S = 1K, R_1 = 50 K, R_2 =2 K, R_C = 1K, R_L = 1.2K, h_{fe} = 50, h_{ie} =1.1K, $h_{re} = h_{oe} = 0$; Find A_I, R_i, R_o, A_V and power gain. [8+8]

2. A two stage FET RC coupled amplifier has the following parameters: $g_m = 10mA/V$, $r_d = 5.5K$ *and* R_g = 0.5 M for each stage. Assume C_S is arbitrarily large.
   (a) What must be the value of C_b in order that the frequency characteristic of each stage be flat within 1 dB down to 10 Hz ?
   (b) Repeat the above part if the overall gain of both stages is to be down 1 dB at 10 Hz.
   (c) What is the overall mid band voltage gain ? [8+4+4]

3. (a) Draw Hybrid - π model of a transistor in CC configuration using CE Hybrid - π parameters.
   (b) Delete all capacitors from the above emitter-follower equivalent circuit and find the input impedance and output impedance. [8+8]

4. (a) Compare the series fed and transformer coupled Class - A power amplifiers. Why is the conversion efficiency doubled in transformer coupled Class-A amplifier? [8]
   (b) Discuss in detail the origin and effect of cross-over distortion. How do you avoid the cross over distortion in power amplifiers circuit? Discuss in detail. [8]

5. (a) Explain what happens to the gain because of the presence of feedback capacitance from collector to base in single tuned BJT amplifier circuit?
   (b) Explain in detail the Unilateralisation technique with the help of circuit diagram?
   (c) Explain the difference between Neutralization and Unilateralisation techniques? [4+8+4]

6. (a) Draw the Gain versus Frequency response of uncompensated and high frequency compensated CE wide band amplifier assuming that the lower 3-dB frequency is zero.

(b) Explain High frequency compensation and what are the methods provided to achieve High frequency compensation in a CE amplifier? [8+8]

7. (a) The voltage regulator in Figure 7a maintains an output voltage of 25 V.
   i. What value of Rsc should be used to limit the maximum current to 0.5A?
   ii. With the value of Rsc found in (i) what will be the output voltage when RL= 100 ohms? When RL =10 ohms?

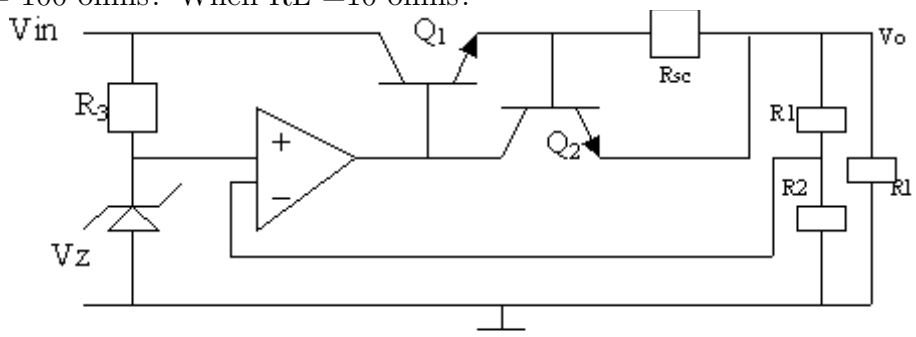

Figure 7a

(b) Draw and explain the regulator which will provide the foldback limiting .[8+8]

8. (a) Draw the block diagram of IC 723 and explain its operating principle.
   (b) Draw and explain the Fullwave voltage Doubler and give its applications. [8+8]

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