SET- 1

Code No: 2420406

IV B. Tech II Semester Regular Examinations, April/May 2009
DSP Processors and Architectures
(Common to E.C.E., E.I.E. &B.M.E)

Time: 3 Hours **Max. Marks 80**

Answer any FIVE questions
All questions carry equal marks
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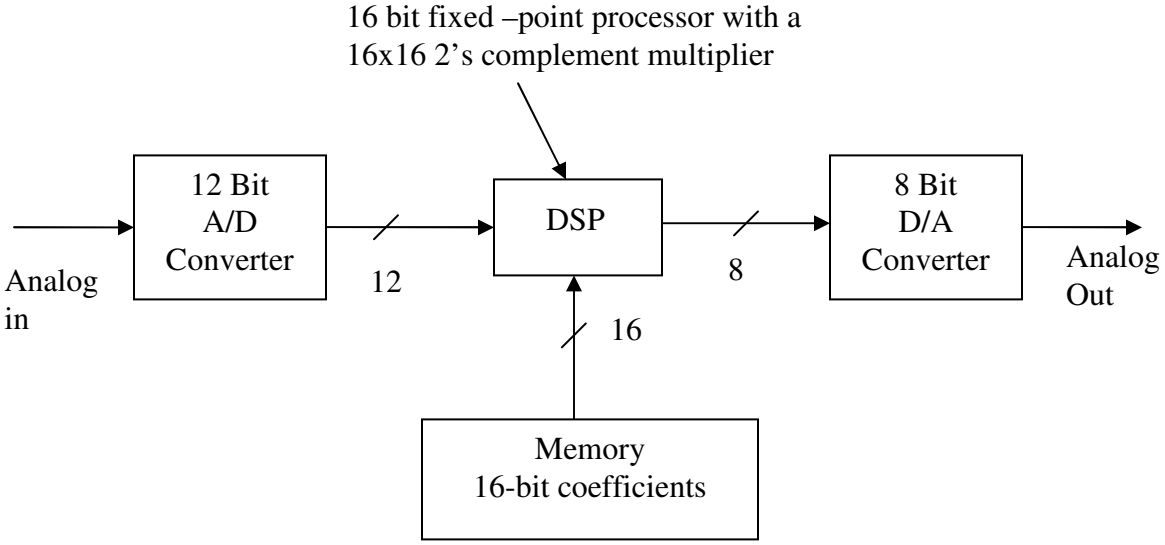
1. a) Find the DFT of the sequence {1, 1, 1, 1, 2, 2 ,2, 2} using radix-2 Decimation – in – Frequency FFT. (12)
   b) Compare FIR and IIR filter. (4)
2. For the DSP system shown in the block diagram, the analog input is a 50Hz sinusoidal signal with 2 V peak value. Both the A/D and D/A converters are 0 – 5 V devices. Determine a) the SNR of A/D b) the SNR of DSP c) the peak output of the D/A converter. Assume a sampling rate of 400 samples/sec. State other assumptions that are needed for calculations.



3. Explain the DSP addressing modes with suitable examples.
4. Explain about different branching effects.

SET- 1

Code No: 2420406

5. a) Write a sequence of TMS320C54xx instructions to configure a circular buffer with a start address at 0200h and an end address at 021fh with current buffer pointer (AR6) pointing to address 0205h.

   b) What will be the contents of accumulator A after the execution of the instruction LD * AR4, 4, A if the current AR4 points to a memory location whose contents are 8b0eh and the SXM bit of the status register STI is set?
6. Determine the linearly interpolated sequence from the given sequence x(n) = [0 4 8 12 16 8 4 0] for an interpolation factor of 3. What interpolating sequence h(n) can achieve the specified interpolation.
7. a) Derive the optimum scaling factor for the DIF FFT butterfly.

   b) What minimum size FFT must be used to compute a DFT of 40 points? What must be done to the samples before the chosen FFT is applied?
8. Design a circuit to interface 64k words of the program memory space from 0FFFFFh to 0F0000h for the TMS320C5416 processor using 16K x 16 memory chips.

SET- 2

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1. a) Find the DFT of the sequence {1, 1, 1, 1, 2, 2, 2, 2} using radix-2 Decimation-in-Time FFT. Sketch the magnitude and phase plot. (12)
   ii) What is the need for FFT? (4)
2. a) Compute the dynamic range and the percentage resolution for a block floating point format with a 4-bit exponent used in a 16-bit fixed point processor. (8)
   b) Show that the dynamic range of a signal increases by 6 db for each additional bit used to represent its value. (8)
3. a) What is the difference between a micro coded program control and a hardwired program control? Why is the later preferred for DSP implementation? (8)
   b) List the major architectural features used in a digital signal processor to achieve high speed of program. (8)
4. What is hardware looping? Explain in detail.
5. Identify the addressing mode of the source operand in each of the following instructions.
   a) ADD *AR2, A
   b) READA *AR2
   c) ADD *AR2+%, A
   d) ADD #0ffh, A
   e) ADD 1234h, A
   f) ADD *AR2+0B, A
   g) ADD *+AR2, A
   h) LD *(1000h), A

SET- 2

Code No: 2420406

6. Represent each of the following as 16 – bit numbers in the desired Q – notation.
   a) 0.3125 as a Q15 number
   b) -0.3125 as a Q15 number
   c) 3.125 as a Q7 number
   d) -352 as a Q0 number
7. Derive equations to implement a butterfly encountered in a DIF FFT implementation. Such a butterfly is represented by the following equations:

$$A_R^{'} + jA_I^{'} = (A_R + jA_I) + (B_R + jB_I)$$

$$B_R^{'} + jB_I^{'} = ((A_R + jA_I) - (B_R + jB_I))(W_R^r + jW_I^r)$$

8. a) What are the various classifications of interrupts for the TMS320C5416 processor?
   b) How does the interrupt handling in the TMS320C54xx DSP differ for a software and a hardware interrupt?

SET- 3

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1. a) The signal sequence x(n) = [0 2 4 6 8] is interpolated using the interpolation filter sequence b_k = [0.5 1 0.5] and the interpolation factor is 2. Determine the interpolated sequence y(n).

   b) Determine the periods for the periodic sequences i) $e^{-jn\pi/8}$ ii) $e^{-jn3\pi/8}$
2. Write about the different sources of error in DSP implementation.
3. a)Explain about multiply and accumulate unit

   b) List the essential peripherals required to implement the following DSP systems.

   i) Speech processing system

   ii) A biomedical instrumentation system

   iii) An image processing system
4. Explain about various pipeline programming models.
5. Explain the various data addressing modes of TMS320C54xx processors with suitable examples.
6. Develop a decimation filter program that can be used to decimate by a factor of 2^5 using a subroutine to decimate by a factor of 2 in conjunction with appropriate filters.
7. Determine the following for a 128-point FFT computation:

   a. number of stages

   b. number of butterflies ion each stage

   c. number of butterflies needed for the entire computation

   d. number of butterflies that need no twiddle factors

   e. number of butterflies that require real twiddle factors

   f. number of butterflies that require complex twiddle factors
8. What is DMA? Explain its role and operation in a DSP processor.

SET- 4

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1. Design and also realize a high pass FIR filter with a cutoff frequency of 1.3 rad/sec and N=9. (16)
2. Write about the different number formats for signals and coefficients in DSP systems.
3. What are the various DSP computational building blocks? Explain any two of them.
4. What is pipelining and explain the different pipeline programming models.
5. Explain the difference between the internal and external modes of clocking TMS320C54xx processors. How do you vary the clock frequency in each case?
6. Implement the IIR filter represented by the following difference equation on the TMS320C54xx. Assume that Q15 notation is used to represent the values of coefficients and Q0 to represent the signal samples.
   $y(n) = b(0)x(n) + b(1)x(n-1) + a(0)y(n-1) + a(1)y(n-2) + a(2)y(n-3)$
7. A time domain sequence of 73 elements is to be convolved with another time domain sequence of 50 elements using DFT to transform the two sequences, multiplying them, and then doing IDFT to obtain the resulting time domain sequence. To implement DFT or IDFT, the DIT-FFT algorithm is to be used. Determine the total number of complex multiplies needed to implement the convolution. Assume that each butterfly computation requires one complex multiplication.
8. a) How does DMA help in increasing the processing speed of a DSP processor?
   b) Write a TMS320C54xx code to initialize the DMA channel 5 destination register to #5555h without using auto increment, Rewrite the code using auto increment for the same operation.