Code No: RR320405 **Set No. 1**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in linear region.
   (b) A PMOS transistor is operating in saturation region with the following parameters. $V_{GS} = -5V$; $V_{tp} = -1.2V$; $W/L = 95$; $\mu nCox = 95\ \mu A/V^2$
   Find Trans conductance of the device. [8+8]

2. With neat sketches explain how Diodes and Resistors are fabricated in Bipolar process. [16]

3. Design a stick diagram for two input n-MOS NAND and NOR gates. [16]

4. Design a layout diagram for nMOS inverter. [16]

5. Calculate ON resistance from V_{DD} to GND for the given inverter circuit shown in Figure 5, If n-channel sheet resistance is $3 \times 10^4 \Omega$ per square. [16]

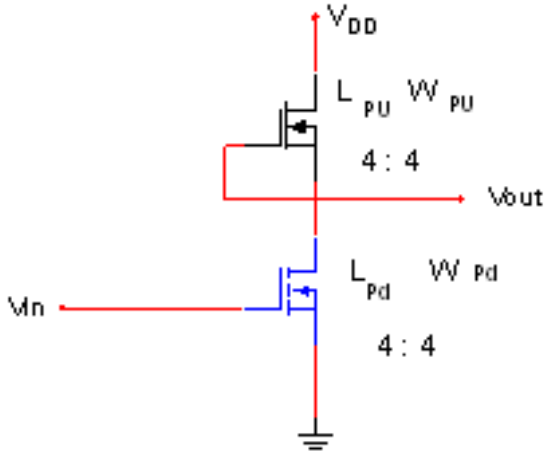

Figure 5

6. Clearly discus about the following FPGA Technology
   (a) Anti fuse Technology.
   (b) Static RAM Technology. [8+8]

7. Explain the following process in the ASIC design flow.
   (a) Functional gate level verification.

(b) Static timing analysis. [8+8]

8. (a) Mention the properties of the twin oxide.
   (b) Clearly explain about ION implantation step in IC fabrication. [6+10]

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Code No: RR320405 **Set No. 2**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With neat sketches explain the formation of the inversion layer in P-channel Enhancement MOSFET.
   (b) An NMOS Transistor is operated in the triode region with the following parameters $V_{GS} = 4V$; $V_{tn} = 1V$; $V_{DS} = 2V$; $W/L = 100$; $\mu nCox = 90\ \mu A/V^2$ Find its drain current and drain source resistance. [8+8]
2. (a) With neat sketches explain how resistors and capacitors are fabricated in p-well process.
   (b) With neat sketches explain how resistors and capacitors are fabricated in n-well process. [8+8]
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(AB + CD)}$ [16]
4. Design a layout diagram for the NMOS logic shown below $Y = \overline{(A + B).C}$ [16]
5. Explain clearly about different parastic capacitances of an nMOS transistor. [16]
6. Implement Full-adder circuit using PAL. [16]
7. What is need for RTL simulation? Clearly explain RTL simulation flow in the ASIC design flow and also mention few leading simulation tools. [16]
8. With neat sketches explain the ION- lithography process. [16]

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Code No: RR320405 **Set No. 3**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) With neat sketches explain the formation of the inversion layer in P-channel Enhancement MOSFET.
   (b) An NMOS Transistor is operated in the triode region with the following parameters $V_{GS} = 4V$; $V_{tn} = 1V$; $V_{DS} = 2V$; $W/L = 100$; $\mu nCox = 90\ \mu A/V^2$ Find its drain current and drain source resistance. [8+8]
2. With neat sketches explain CMOS fabrication using Twin - Tub process. [16]
3. Design a stick diagram for the PMOS logic shown below $Y = \overline{(AB + CD)}$ [16]
4. Design a layout diagram for two input nMOS NAND gate. [16]
5. Two nMOS inverters are cascaded to drive a capacitive load C_L=16Cg as shown in Figure 5. Calculate the pair delay Vin to Vout in terms of τ for the given data.
   Inverter -A
   $L_{P.U}$= 16λ , $W_{P.U}$ = 2 λ , $L_{P.d}$ = 2 λ , $W_{P.d}$ = 2 λ
   Inverter -B
   $L_{P.U}$= 2λ , $W_{P.U}$ = 2 λ , $L_{P.d}$ = 2 λ , $W_{P.d}$ = 8 λ [16]

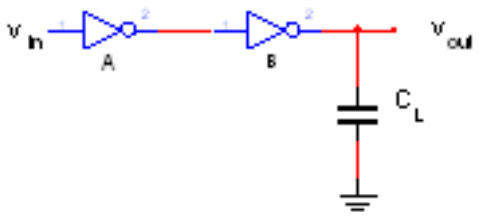

Figure 5

6. Clearly discus about the following FPGA Technology
   (a) Anti fuse Technology.
   (b) Static RAM Technology. [8+8]
7. Explain the following process in the ASIC design flow.
   (a) Functional gate level verification.
   (b) Static timing analysis. [8+8]
8. (a) Mention the properties of the twin oxide.

(b) Clearly explain about ION implantation step in IC fabrication. [6+10]

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Code No: RR320405 **Set No. 4**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive an equation for I_{DS} of an n-channel Enhancement MOSFET operating in linear region.
   (b) A PMOS transistor is operating in saturation region with the following parameters. $V_{GS} = -5V$; $V_{tp} = -1.2V$; $W/L = 95$; $\mu nCox = 95\ \mu A/V^2$
   Find Trans conductance of the device. [8+8]
2. (a) Compare between CMOS and bipolar technologies.
   (b) With neat sketches explain nMOS fabrication process. [8+8]
3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(A+B).C}$ [16]
4. Design a layout diagram for two input CMOS NOR gate. [16]
5. Calculate ON resistance from V_{DD} to GND for the given inverter circuit shown in Figure 5, If n-channel sheet resistance is $3 \times 10^4 \Omega$ per square. [16]

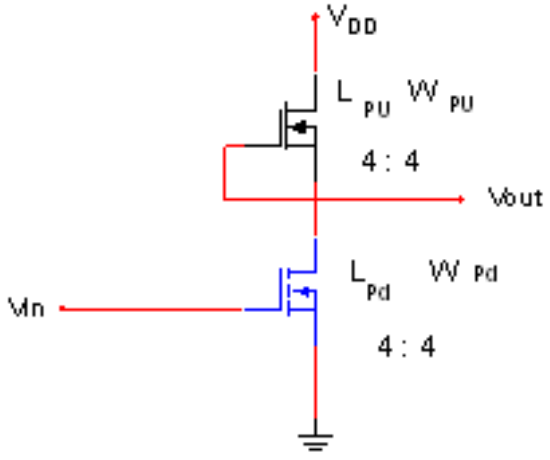

Figure 5

6. With neat sketch clearly explain the architecture of a PLA. [16]
7. (a) What is the goal of VHDL synthesis step in design flow?
   (b) Explain how register transfer level description provides optimized synthesis netlist. [8+8]
8. With neat sketches explain the ION- lithography process. [16]

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