III B.Tech II Semester Regular Examinations, Apr/May 2007
VLSI DESIGN
(Common to Electronics & Communication Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Derive an equation for Transconductance of an n-channel enhancement MOSFET operating in Active region.

   (b) For the arrangement shown below plot the on-resistance of M as a function of V$_G$. Assume $V_{tn} = 0.7$ V; W/L = 10; μnCox = 50μA/V^2
   Note the drain terminal is open. (Figure 1b)

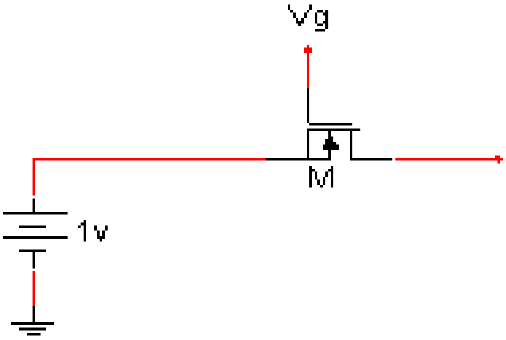

Figure 1b

[10+6]

2. With neat sketches explain how npn transistor is fabricated in Bipolar process. [16]

3. What is a stick diagram and explain about different symbols used for components in stick diagram. [16]

4. Design a layout diagram for two input pMOS NAND gate. [16]

5. Calculate ON resistance from V$_{DD}$ to GND for the given inverter circuit shown in Figure 5. If n-channel sheet resistance is $2 \times 10^4\Omega$ per square. [16]

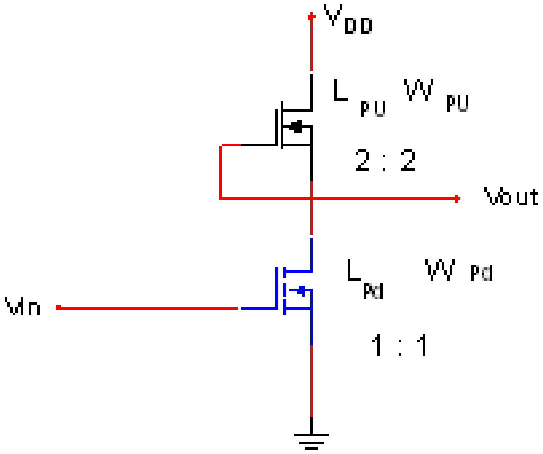

Figure 5

6\. (a) What are the advantages and disadvantages of the reconfiguration.

(b) Mention different advantages of Anti fuse Technology. [8+8]

7\. What is need for RTL simulation? Clearly explain RTL simulation flow in the ASIC design flow and also mention few leading simulation tools. [16]

8\. With neat sketches explain the ION- lithography process. [16]

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Code No: RR320405 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Find g_m and r_{ds} for an n-channel transistor with $V_{GS} = 1.2V$; $V_{tn} = 0.8V$; W/L = 10; μnCox = 92$\mu A/V^2$and V_{DS} = Veff. The out put impedance constant. $\lambda = 95.3 \times 10^{-3} V^{-1}$
   (b) Define the term Threshold voltage of MOSFET and explain its significance. [10+6]

2. (a) With neat sketches explain how resistors and capacitors are fabricated in p-well process.
   (b) With neat sketches explain how resistors and capacitors are fabricated in n-well process. [8+8]

3. Design a stick diagram for the CMOS logic shown below $Y = \overline{(AB + CD)}$ [16]

4. Explain with suitable examples how design the layout of a gate to maximize performance and minimize area. [16]

5. Calculate on resistance of the circuit shown in Figure 5 from V_{DD} to GND. If n-channel sheet resistance Rsn = $10^{\ 4}$ Ω per square and p-channel sheet resistance $Rsp = 2.5 \times 10^4 \Omega$ per square. [16]

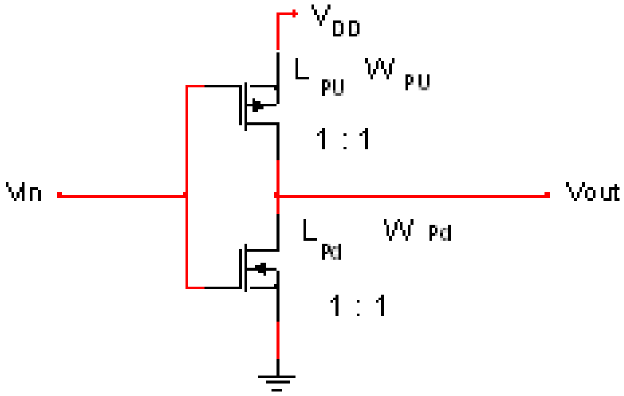

Figure 5

6. (a) What are the advantages and disadvantages of the reconfiguration.
   (b) Mention different advantages of Anti fuse Technology. [8+8]

7. Clearly explain each step of high level design flow of an ASIC. [16]

8. Explain about the following two oxidation methods.
   (a) High pressure oxidation.
   (b) Plasma oxidation. [8+8]

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1. (a) Clearly explain the body effect of the MOSFET.
   (b) Clearly explain about channel length modulation of the MOSFET. [8+8]
2. With neat sketches explain how Diodes and Resistors are fabricated in pMOS process. [16]
3. Design a stick diagram for n-MOS Ex-NOR gate. [16]
4. Design a layout diagram for CMOS inverter. [16]
5. Derive an equation for the propagation delay from input to output of the pass transistor chain shown in Figure 5. [16]

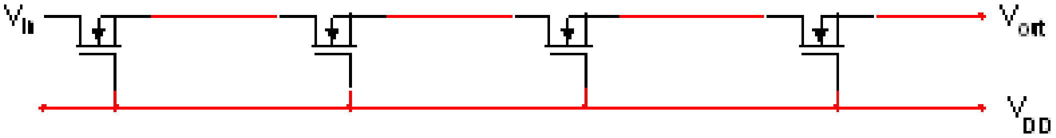

Figure 5

6. (a) What are the advantages and disadvantages of the reconfiguration.
   (b) Mention different advantages of Anti fuse Technology. [8+8]
7. (a) What are the different constraints that are passed to the synthesis tool in the synthesis step of the ASIC design and clearly discuss about these constraints.
   (b) Mention different report files that are generated by the synthesis tool and discuss clearly about each report file. [8+8]
8. With neat sketches explain the oxidation process in the IC fabrication process. [16]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Define threshold voltage of a MOS device and explain its significance.
   (b) Explain the effect of threshold voltage on MOSFET current Equations. [8+8]
2. With neat sketches explain how Diodes and Resistors are fabricated in Bipolar process. [16]
3. Design a stick diagram for two input p-MOS NAND and NOR gates. [16]
4. Design a layout diagram for two input CMOS NOR gate. [16]
5. Two nMOS inverters are cascaded to drive a capacitive load C_L=16Cg as shown in Figure 5. Calculate the pair delay Vin to Vout in terms of τ for the given data.

   Inverter -A

   $L_{P.U} = 16\lambda$, $W_{P.U} = 2\ \lambda$, $L_{P.d} = 2\ \lambda$, $W_{P.d} = 2\ \lambda$

   Inverter -B

   $L_{P.U} = 2\lambda$, $W_{P.U} = 2\ \lambda$, $L_{P.d} = 2\ \lambda$, $W_{P.d} = 8\ \lambda$ [16]

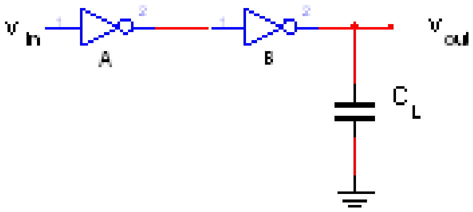

Figure 5

6. With neat sketches explain the architecture of PAL. [16]
7. What is need for RTL simulation? Clearly explain RTL simulation flow in the ASIC design flow and also mention few leading simulation tools. [16]
8. Explain about the following two oxidation methods.
   (a) High pressure oxidation.
   (b) Plasma oxidation. [8+8]

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