Code No: RR320501 **Set No. 1**

III B.Tech II Semester Supplimentary Examinations, Aug/Sep 2007
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Distinguish between multiprogramming and time-sharing systems. It is said although all time-sharing systems are multiprogramming systems all multiprogramming systems need not necessarily be time sharing systems. Comment on this statement. [16]

2. (a) Derive the expressions for efficiency, throughput and speed up for k stage pipeline for n tasks.
   (b) What are key issues in the design of an efficient dynamic pipeline processor. [8+8]

3. (a) What are the routing functions used by shuffle exchange network? Compare with shifter.
   (b) Explain the action of the action of Perfect and Inverse Perfect shuffle for N = 8.
   (c) What is the difference between Omega and repositioned Omega network and how repositioning network is advantages? [4+8+4]

4. (a) Discuss the steps involved in M(j,2) sorting algorithm.
   (b) Describe Bit parallel Associative memory organization with suitable diagram. [8+8]

5. (a) Give the architecture of K-map in Cm* architecture. With a diagram explain how an intracluster memory access is performed?
   (b) What is a cluster? How communication is possible between clusters? Explain. [8+8]

6. (a) Explain performance tradeoffs in memory organizations.
   (b) How caches can be associated with shared memory? How this configuration avoids cache coherence. [8+8]

7. (a) Describe data flow design alternatives.
   (b) Explain the organization of the EDDY data flow machine. [8+8]

8. (a) Explain the staging memory concept in MPP and instruction set of the MPP.
   (b) How new image processing techniques are developed using MPP. [8+8]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) What are the different types of memories that are present in a memory hierarchy? Describe the characteristics of each of these memories.
   (b) What is meant by interleaving memory addresses? Describe the different ways of implementing interleaving schemes. Illustrate with the help of proper diagrams. What are the relative merits and demerits of these schemes? [8+8]
2. (a) What are pipeline hazards? What are the causes of pipeline hazards? Describe briefly the hazard detection and resolution of hazards in pipelines.
   (b) What are the various classes of data-dependant hazards? Describe the hazards and their removal. [8+8]
3. (a) Discuss the various types of structures used in a Network Construction.
   (b) Give the advantages and disadvantages of Multistage Networks over Single Stage Networks. [8+8]
4. (a) Compare the two types of Associative Processor organizations.
   (b) Differentiate between Bit-slice and Word-slice operations in STARAN. [10+6]
5. (a) With a diagram explain the construction of 4^2X3^2 Delta network.
   (b) Compare and contrast the performance of interconnection networks. [10+6]
6. (a) Define the term nonpreemptive scheduling. With an example illustrate the Hu's optimal algorithm.
   (b) Explain briefly a simple queueing model for multiprocessor scheduling.[10+6]
7. (a) Describe the instruction execution process in a data flow computer for computation of a = (b+1)*(b-c) .
   (b) Describe VLSI matrix multiplication. [8+8]
8. (a) Give the features of Hydra operating system.
   (b) Demonstrate the effect of memory contention on the performance of C.mmp. [8+8]

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Code No: RR320501 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Briefly explain the characteristics of memory devices in a memory hierarchy what is memory interleaving?
   (b) Differentiate between high-order and low-order memory interleaving. [8+8]
2. (a) With the help of neat block diagram explain the concept of Linear pipe line, and how it differs with non linear pipe line.
   (b) Design a Linear pipe line for a Floating Point Adder. [8+8]
3. (a) Discuss the issues involved for Inter− PE Communication in array processors.
   (b) What is a Multistage Network? Describe different types of multistage network. [8+8]
4. (a) How is the Summation functionality performed in a SIMD Machine?
   (b) Name some SIMD parallel algorithms and along with their complexity.
   (c) What is the motivation of an Array Processor? [10+4+2]
5. (a) Explain the desirable characteristics of interconnection networks for Multiprocessor environment.
   (b) Explain a master-slave configuration of the PDP-10 Multiprocessor system. [8+8]
6. (a) Compare three operating system configurations for multi processor computer.
   (b) Explain various operating system requirements for multiprocessor computers. [8+8]
7. (a) Describe any four systolic array configurations.
   (b) Describe how algorithms are mapped into VLSI arrays. [8+8]
8. (a) Demonstrate the effect of different synchronization mechanisms on the performance of C.mmp.
   (b) Describe the functional structure of a computer module in the C.mmp. [8+8]

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Code No: RR320501 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Draw the structure of a parallel memory system with consecutive words in a module and describe its working. Also highlight its merits and demerits.
   (b) Draw the structure of a parallel memory system with consecutive words in consecutive modules and describe its working. Also highlight its merits and demerits. [8+8]

2. (a) Describe the effect of conditional statements on pipeline processes Suggest improvements.
   (b) Explain how Data Buffering and Busing Structures improves efficiency of pipeline processors. [8+8]

3. Design a data routing Network for an SIMD Array processor with 256 $PE's$. Draw an interconnection Barrel shifting network showing all directly wired connections among the 256 $PE's$ and calculate the minimum number of routing steps from any PE_I to any otherPE_{I+k} for the arbitrary distance $1 \leq k \leq 255$. [16]

4. Discuss sorting patterns with respect to three ways of indexing the$PE's$. [16]

5. (a) Explain the Cm* architecture for a hierarchical loosely coupled system and explain the steps involved in an intracluster memory access.
   (b) List the advantages and disadvantages of asymmetric and symmetric I /O systems in a multiprocessor system. [12+4]

6. (a) Describe multicache problems? Describe methods to solve these problems.
   (b) Describe a methodology to evaluate different multiprocessor memory configurations. [8+8]

7. (a) Compare Control flow computers against Data flow computers.
   (b) Explain with an example, how an instruction is executed in a data flow computer. [8+8]

8. (a) Give the Inter CPU Communication structure of Cray X-MP System.
   (b) Describe the functions of solid state storage device of the I/O Sub system of a Cray X-MP. [8+8]

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