Code No: RR320501 **Set No. 1**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Describe the Handler's classification of pipeline processors.
   (b) Describe the approaches at can enhance the vector processing capability. [8+8]
2. (a) With the help of neat block diagram explain the concept of Linear pipe line, and how it differs with non linear pipe line.
   (b) Design a Linear pipe line for a Floating Point Adder. [8+8]
3. (a) What are the parameters that characteristics SIMD computers ?
   (b) What is masking. Explain masking mechanism.
   (c) Analyse the various components in a Processing Element of an array processor. [5+6+5]
4. (a) How is the Summation functionality performed in a SIMD Machine?
   (b) Name some SIMD parallel algorithms and along with their complexity.
   (c) What is the motivation of an Array Processor? [10+4+2]
5. (a) Explain a symmetric configuration of the PDP-10 Multiprocessor system.
   (b) Explain the process of context switching in a Processor with multiple register sets. [10+6]
6. (a) Write a parallel algorithm to implement a concurrent quick sort algorithm.
   (b) Explain various cache coherence and synchronization mechanisms. [8+8]
7. (a) Describe the properties of data flow languages.
   (b) Draw a data flow graph to represent z = N!. [8+8]
8. (a) Give the characteristics of the Cray-1 computer system.
   (b) Explain with neat diagrams the 4 types of vector instruction in Cray and give example. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR320501 **Set No. 2**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain the hierarchical memory system and how this concept is used to implement parallel processing.
   (b) What is Balancing of subsystem Band width? Explain how the different balancing techniques improve the parallelism? [8+8]
2. (a) Design a pipelined instruction unit.
   (b) With suitable diagrams explain non-linear pipelining and give the significance of reservation table. [8+8]
3. (a) Construct of mesh connected an ILLiac-IV Network with N = 16 PE's. What is its equivalent chordal ring topology.
   (b) List down the various routing functions that characterizes Illiac $-$IV Network. [8+8]
4. Discuss sorting patterns with respect to three ways of indexing the$PE's$. [16]
5. (a) What is a banyan network ? Explain the derivation of a (2,2,2) banyan network from the two-level binary tree. Also mention the advantage of this network
   (b) Describe the following IN's associated with a Multiprocessor system
      i. Crossbar switches.
      ii. Multiport memory.
   (c) Discuss how 1-by-8 demultiplexer is implemented with 2x2 switch boxes. [8+6+2]
6. Explain briefly how to exploit concurrency in Multiprocessors. [16]
7. (a) Describe the instruction execution process in a data flow computer for computation of a = (b+1)*(b-c) .
   (b) Describe VLSI matrix multiplication. [8+8]
8. (a) Demonstrate the effect of different synchronization mechanisms on the performance of C.mmp.
   (b) Describe the functional structure of a computer module in the C.mmp. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR320501 **Set No. 3**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What are interleaved memory organizations? What are the considerations in choosing these memory organizations for pipeline or vector processors?
   (b) Explain the S-access memory organization for pipeline vector processors with the help of neat diagrams depicting the configuration and the timing diagram of the configuration. [8+8]
2. (a) What is the utility of a reservation table? Taking a suitable unifunction pipeline as an example, draw the reservation table and its state diagram.
   (b) What are reconfigurable pipelines? Explain the benefit of these pipelines with the help of a suitable example. [8+8]
3. (a) Discuss the issues involved for Inter− PE Communication in array processors.
   (b) What is a Multistage Network? Describe different types of multistage network. [8+8]
4. Explain the following terminologies associated with SIMD computers
   (a) Lock-step Operations.
   (b) Associative Memory.
   (c) Adjacency search.
   (d) Bit serial Associative Processor. [16]
5. (a) With a diagram explain the construction of 4^2X3^2 Delta network.
   (b) Compare and contrast the performance of interconnection networks. [10+6]
6. (a) Explian about static coherence check and dynamic coherence check.
   (b) Explain the functions of fork and join and cobegin and coend with relevant examples. [8+8]
7. (a) Explain the organization of a dynamic data flow computer.
   (b) What is data flow graph? Explain how a data flow graph constructed. [8+8]
8. (a) Explain the staging memory concept in MPP and instruction set of the MPP.
   (b) How new image processing techniques are developed using MPP. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: RR320501 **Set No. 4**

III B.Tech II Semester Supplimentary Examinations, Apr/May 2008
ADVANCED COMPUTER ARCHITECTURE
(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Explain the fast computation applications in the following areas.
   (a) Energy Resources exploration.
   (b) Medical, Military and Basic Research. [8+8]
2. (a) Derive the expressions for efficiency, throughput and speed up for k stage pipeline for n tasks.
   (b) What are key issues in the design of an efficient dynamic pipeline processor. [8+8]
3. How many steps are required to broadcast an information item from one PE to other$PE's$ in the following single stage interconnection Networks with $2^n PE's$.
   (a) Shuffle Exchange network.
   (b) A Cube Network. [16]
4. (a) What is an associative memory? Discuss a simple associative memory organization with suitable diagrams.
   (b) Explain the architecture of PEPE association processor. [8+8]
5. (a) Compare the performance of three multiprocessor interconnection structures.
   (b) Explain briefly multiport memory organization with private memories. [10+6]
6. (a) Explian about static coherence check and dynamic coherence check.
   (b) Explain the functions of fork and join and cobegin and coend with relevant examples. [8+8]
7. (a) Explain the organization of a static data flow computer.
   (b) What are the major design issues of a data flow computer? Explain in detail. [8+8]
8. (a) What are the 3 sections which characterize the Cray − I computer system and explain each section with diagrams.
   (b) What are the functional pipeline units in Cray − I. Explain the concept of pipeline chaining and vector loops. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆