Code No: R05410207 **Set No. 1**

IV B.Tech I Semester Regular Examinations, November 2008
VLSI DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Explain the following terms related to the fabrication of IC
   (a) Diffusion
   (b) oxidation
   (c) Lithography
   (d) Metallization. [4+4+4+4]
2. (a) With neat sketches, explain the transfer characteristic of a CMOS inverter.
   (b) Derive an equation for I_{ds} of an n-channel enhancement MOSFET operating in saturation region. [8+8]
3. Implement following logic functions using CMOS logic
   (a) $\overline{(A+B)\,C}$
   (b) $\overline{((AB+C)\,D)}$. [8+8]
4. (a) Explain the concept of sheet resistance and apply it to compute the ON resistance (V_{DD} to GND) of an NMOS inverter having pull up to pull down ratio of 4:1, If n channel resistance is $R_{sn} = 10^4\ \Omega$ per square.
   (b) Calculate the gate capacitance value of 5μm technology minimum size transistor with gate to channel capacitance value is $4 \times 10^{-4} pF/\mu m^2$. [10+6]
5. (a) Compare different types of CMOS subsystem Adders.
   (b) Draw the mask layout for 6 transistor static RAM used in ASIC memories. [8+8]
6. (a) Draw and explain the Antifuse Structure for programming the PAL device.
   (b) Explain how the I/O pad is programmed in FPGA. [8+8]
7. (a) How to avoid a floating nodes in a multiplexer and write corresponding VHDL program.
   (b) Draw a typical schematic and schematic icon for a module and what are additional operations are added to the electrical nature of it. [8+8]
8. Explain the following with respect to CMOS testing: [4×4=16]

(a) ATPG
(b) Fault simulation
(c) Statistical Fault Analysis
(d) Fault Sampling.

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Code No: R05410207 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Briefly discuss the steps involved in the manufacturing process of an IC. [16]
2. (a) Clearly explain the body effect of a MOS FET.
   (b) Clearly explain channel length modulation of a MOS FET. [8+8]
3. Design a stick diagram for the N MOS logic shown below. Draw the circuit diagram and layout
   $Y = \overline{(A + B + C)}$. [16]
4. Describe three sources of wiring capacitances. Explain the effect of wiring capacitance on the performance of a VLSI circuit. [16]
5. (a) Draw the schematic for Transmission gate adder and explain its operation with truth table.
   (b) Show the basic one row and one column RAM architecture and explain its operation. [8+8]
6. (a) What are different classes of Programmable CMOS devices? Explain them briefly.
   (b) What is the basis for standard-cell? What are basic classes of circuits for Library cells? [8+8]
7. (a) Compare the Hardware and Software Languages.
   (b) Draw the basic design flow through typical CMOS VLSI tools and give some names of corresponding tools. [8+8]
8. (a) Explain how the cost of chip can effect with the testing levels,
   (b) Explain how observability is used to test the output of a gate within a larger circuit.
   (c) How the Iterative Logic Array Testing can be reduced number of tests. [5+6+5]

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Code No: R05410207 **Set No. 3**

IV B.Tech I Semester Regular Examinations, November 2008
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. Describe Ion implantation mechanism in IC fabrication. [16]
2. (a) Discuss the gate source and gate drain capacitance of an nFET.
   (b) Calculate the gate capacitance of an nFET with following parameter. W=8μm, L=0.5μm, $C_{ox} = 3.45 \times 10^{-7} F/cm^2$. [8+8]
3. (a) Distinguish between RTL Simulation and RTLSynthesis.
   (b) Explain the place and route tools used in VLSI design flow. [8+8]
4. Explain the following:
   (a) The delay unit.
   (b) Inverter delays. [8+8]
5. (a) Design a comparator using XNOR and AND gate and draw its schematic.
   (b) Design a zero/one detector and draw its schematic and also calculate its delay. [8+8]
6. (a) Draw the diagram of programmed I/O pad and explain how the antifuses are used in this.
   (b) Draw and explain the AND/OR representation of PLA. [8+8]
7. (a) Write a VHDL program for 7-sengment display decoder.
   (b) What are the basic sources of errors in CMOS circuits and how these are tested? Give name of such a simulator. [8+8]
8. (a) What type of defects are tested in manufacturing testing methods?
   (b) What is the Design for Autonomous Test and what is the basic device used in this?
   (c) What type of tests are used to check the noise margin for CMOS gates? [4+6+6]

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Code No: R05410207 **Set No. 4**

IV B.Tech I Semester Regular Examinations, November 2008
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What are the advantages of BICMOS Technology over CMOS Technology?
   (b) Explain how a bipolar NPN transistor is included in N well CMOS processing. Draw the cross section of BICMOS transistor. [4+12]

2. (a) What is body affect? Discuss different parameters on which threshold voltage depends?
   (b) Determine Z_{pu} to Z_{pd} ratio for nMOS inverter driven through one or more pass transistor? [8+8]

3. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
   (b) What are the effects of scaling on V_t?
   (c) What are design rules? Why is metal- metal spacing larger than poly -poly spacing. [8+4+4]

4. Two nMOS inverters are cascaded to drive a capacitive load C_L=16 $\square C_g$. Calculate the pair delay (V_{in} to V_{out}) in terms of τ for the inverter geometry indicated in figure 4. What are the ratios of each inverter? If strays and wiring are allowed for,it would be reasonable to increase the capacitance to ground across the output of each inverter by 4 $\square C_g$. What is the pair delayallowing for strays? Assume a suitable value for τ and evaluate this pair delay. [16]
   Inverter 1 $L_{pu} = 16\lambda$, $W_{pu} = 2\lambda$, $L_{pd} = 2\lambda$,$W_{pd} = 2\lambda$
   Inverter 2 $L_{pu} = 2\lambda$,$W_{pu} = 2\lambda$, $L_{pd} = 2\lambda$, $W_{pd} = 8\lambda$

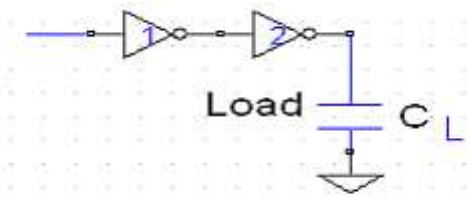

Figure 4

5. Develop a model of word line decoder delay for a RAM with 2^n rows and 2^m columns. Assume true and complementary inputs are available and that the input capacitance equals the capacitance of one of the columns of H=2^m. Use static CMOS gates and express result in terms of n and m. [16]

6. (a) What are different classes of Programmable CMOS devices? Explain them briefly.
   (b) What is the basis for standard-cell? What are basic classes of circuits for Library cells? [8+8]

7. (a) Write a VHDL program in behavioral modeling with concurrent signal assignment.
   (b) Explain the method of switch-level simulation for CMOS circuits and name such a simulators. [8+8]

8. (a) Explain the manufacturing test of a chip with suitable examples.
   (b) Explain how an Ad-hoc test technique used to test long counters. [8+8]

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