Code No: R05410508 **Set No. 1**

IV B.Tech I Semester Regular Examinations, November 2008
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Define wall-clock time.
   (b) Give a brief note on:
      i. Desktop Branch mark
      ii. Server Branch mark [8+8]
2. (a) What are the reasons for emergence of general purpose registers?
   (b) Distinguish between little endian and big endian format? [8+8]
3. Explain data dependent hazard with example? [16]
4. What is meant by trace scheduling? Explain in detail? [16]
5. (a) Give the types of "Conflict misses".
   (b) Which principle of locality does the first miss rate reduction technique address? Explain why? [8+8]
6. (a) Give the reasons why cache coherence is an accepted requirement in small scale multiprocessors?
   (b) Draw the state transition diagram for an individual cache block in a directory based system. [8+8]
7. (a) What is the average time to read or write a 512 bytes sector for a disk? The advertised average seek time is 5ms, the transfer rate is 40MB/sec, it rotates at 10,000RPM, and the controller overhead is 0.1ms. Assume the disk is idle so that there is no queuing delay. In addition, calculate the time assuming the advertised seek time is 3 times longer than the measured seek time.
   (b) Write about
      i. Optical Disk
      ii. Magnetic Tapes. [8+8]
8. (a) Define effective bandwidth and derive a formula for it.
   (b) Plot the effective bandwidth versus message size for overheads of 25 and 250 ms and for network banwidths of 100,1000 and 10,000 bits/sec. Vary message size from 16bytes to 4MB. For what message sizes is the effective bandwidth virtually the same as the raw network bandwidth? If overhead is 250ms, for what message sizes is the effective bandwidth always less than 100M bits/sec? [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R05410508 **Set No. 2**

IV B.Tech I Semester Regular Examinations, November 2008
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain Amdhal's law?
   (b) Find the number of dies for 30 cm wafer for a die that is 0.7cm on a side.[8+8]
2. (a) Write a detailed notes on register-memory architecture.
   (b) Discuss in brief about big endian format? [12+4]
3. Explain data dependent hazard with example? [16]
4. What is meant by trace scheduling? Explain in detail? [16]
5. (a) Give the three categories of cache organizations based on the block placement.
   (b) Discribe the block, when it is found in the cache? [8+8]
6. (a) Explain how coherence and consistence are complementary.
   (b) Briefly explain about cache coherence protocols. [8+8]
7. (a) What do you mean by the "hot swapping"?
   (b) Explain "mirroring".
   (c) Explain the block interleaved parity and distributed block interleaved parity. [6+5+5]
8. What is a cluster? Explain about the designing of a cluster with an example. [16]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R05410508 **Set No. 3**

IV B.Tech I Semester Regular Examinations, November 2008
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. Write short notes on:
   (a) TCP Benchmark.
   (b) Learning curves. [8+8]
2. (a) Define Position independence? Explain.
   (b) Discuss the role of a compiler? [8+8]
3. Explain instruction level parallelism. What are the limitations of ILP? [16]
4. Explain pipeline scheduling in detail. [16]
5. (a) Give the three categories of cache organizations based on the block placement.
   (b) Discribe the block, when it is found in the cache? [8+8]
6. (a) On what problem sizes the performance of scientific technical workload is measured. Explain.
   (b) What factors contribute to L3 cache miss rate and how do they change as the L3 cache grows? [8+8]
7. Write about
   (a) Magnetic disk
   (b) Optical Disk
   (c) Magnetic Tapes. [6+5+5]
8. (a) Write short notes on:
      i. Fibre optic Components
      ii. Fibre Optic Cables
      iii. Wavelength division multiplexing.
   (b) Briefly Write about the performance parameters of interconnection networks. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R05410508 **Set No. 4**

IV B.Tech I Semester Regular Examinations, November 2008
ADVANCED COMPUTER ARCHITECTURE
(Computer Science & Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Define learning curve. Explain?
   (b) Explain the need for parallelism. [8+8]
2. Write short notes on:
   (a) Strided addressing.
   (b) Little endian and big endian formats. [8+8]
3. Explain data dependent hazard with example? [16]
4. (a) What are the limitations of conditional or predicated instructions?
   (b) Give a brief note on local scheduling. [8+8]
5. (a) What are fully associative caches? Explain how they are used in calculating capacity misses?
   (b) Define pseudoset .How does the pseudoassociative cache works. [8+8]
6. (a) Mention the two groups of MIMD computers and explain.
   (b) Give the advantages of shared memory organization. [8+8]
7. (a) What is the average time to read or write a 512 bytes sector for a disk? The advertised average seek time is 5ms, the transfer rate is 40MB/sec, it rotates at 10,000RPM, and the controller overhead is 0.1ms. Assume the disk is idle so that there is no queuing delay. In addition, calculate the time assuming the advertised seek time is 3 times longer than the measured seek time.
   (b) Write about
      i. Optical Disk
      ii. Magnetic Tapes. [8+8]
8. Discuss about the practical issues for commercial interconnection networks? [16]

⋆ ⋆ ⋆ ⋆ ⋆