Code No: 07A3EC03 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2008
SWITCHING THEORY AND LOGIC DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Bio-Medical Engineering, Electronics & Control Engineering, Electronics & Computer Engineering and Instrumentation & Control Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) What is the Gray code? What are the rules to construct Gray code? Develop the 4 bit Gray code for the decimal 0 to 15.
   (b) List the XS3 code for decimal 0 to 9.
   (c) What are the rules for XS3 addition? Add the two decimal numbers 123 and 658 in XS3 code. [8+2+6]
2. (a) State Duality theorem. List Boolean laws and their Duals.
   (b) Simplify the following Boolean functions to minimum number of literals:
      i. F = ABC + ABC' + A'B
      ii. F = (A+B)' (A'+B').
   (c) Realize XOR gate using minimum number of NAND gates. [8+4+4]
3. Simplify the following Boolean expressions using K-map and implement them using NOR gates:
   (a) F (A, B, C, D) = AB'C' + AC + A'CD'
   (b) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ. [16]
4. (a) Design BCD to Gray code converter and realize using logic gates.
   (b) Design 2*4 decoder using NAND gates. [10+6]
5. (a) Draw the basic macro cell logic diagram and explain.
   (b) Explain the general CPLD configuration with suitable block diagram. [16]
6. (a) Draw the logic diagram of a 4 bit binary ripple counter using positive edge triggering.
   (b) Draw the block diagram of a 4 - bit serial adder and explain its operation.[16]
7. (a) Write the differences between Mealy and Moore type machines.
   (b) A sequential circuit has 2 inputs w_1=w_2 and an output z. It's function is to compare the i/p sequence on the two i/p's. If w_1=w_2 during any four consecutive clock cycles, the circuit produces z=1 otherwise z=0
   w_1= 0110111000110
   w_2= 1110101000111
   z=0000100001110 [8+8]

8. (a) For the given control state diagram obtain its equivalent ASM chart.
   (b) Design control logic circuit as shown in figure 8b using multiplexers. [8+8]

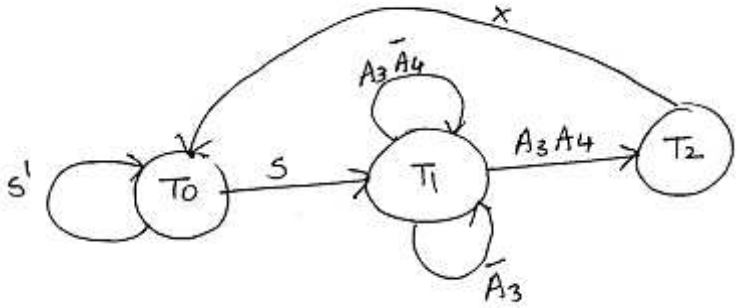

Figure 8b

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Code No: 07A3EC03 **Set No. 2**

II B.Tech I Semester Regular Examinations, November 2008
SWITCHING THEORY AND LOGIC DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Why the binary number system is used in computer design?
   (b) Given the binary numbers
   a = 1010.1, b = 101.01, c =1001.1 perform the following:
      i. a + c
      ii. a - b
      iii. a . c
      iv. a / b.
   (c) Convert (2AC5.D)16 to binary and then to octal. [2+10+4]

2. (a) Simplify the following Boolean functions to minimum number of literals:
      i. (a + b)' (a' + b')'
      ii. y(wz' + wz) + xy
   (b) Prove that AND-OR network is equivalent to NAND-NAND network.
   (c) State Duality theorem. List Boolean laws and their Duals. [4+4+8]

3. (a) What are don't-care conditions? Explain its advantage with example.
   (b) Simplify the following Boolean function for minimal POS form using K-map and implement using NOR gates.
   F(W,X,Y,Z) = π(4,5,6,7,8,12) . d(1,2,3,9,11,14) [4+12]

4. (a) Design BCD to Gray code converter and realize using logic gates.
   (b) Design 2*4 decoder using NAND gates. [10+6]

5. (a) Using PLA logic, implement a BCD to excess 3 code converter. Draw its truth table and logic diagram.
   (b) Disucss about types of sequential PCDs. [16]

6. (a) What do you mean by triggering. Explain the various triggering modes with examples.
   (b) Draw the logic diagram of a JK flip flop and using excitation table, explain its operation. [16]

7. (a) Derive a circuit that realises the FSM defined by the state assigned table in figure below using JK flip flops.

Present State	Next state w=0	Next state w=1	Output
y_2y_1	y_2y_1	y_2 y_1	Z
00	10	11	0
01	01	00	0
10	11	00	0
11	10	01	1

(b) Find the state table for the following state diagram as shown in figure 7b of a simple sequential ckt. [8+8]

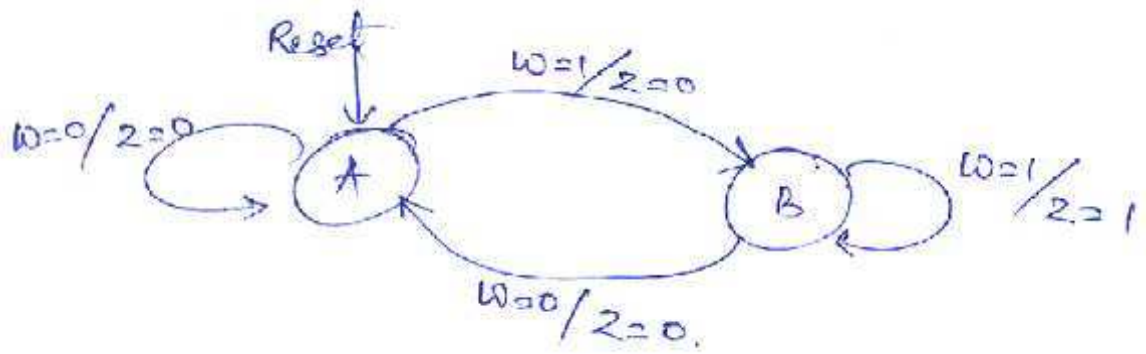

Figure 7b

8. (a) For the given control state diagram, draw the equivalent ASM chart as shown in figure 8a.

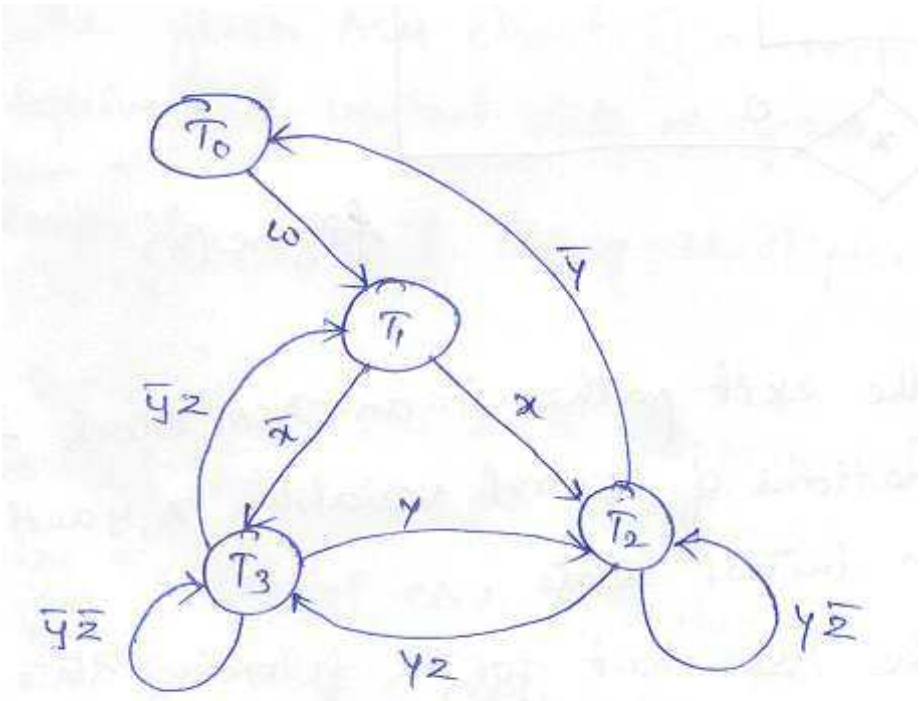

Figure 8a

(b) Design the control circuit using multiplexers for the above state diagram.[8+8]

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Code No: 07A3EC03 **Set No. 3**

II B.Tech I Semester Regular Examinations, November 2008
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What is the necessity of binary codes in computers?
   (b) Encode the decimal numbers 0 to 9 by means of the following weighted binary codes.
      i. 8 4 2 1
      ii. 2 4 2 1
      iii. 6 4 2 -3
   (c) Determine which of the above codes are self complementing and why?[2+12+2]
2. (a) List the Minterms and Maxterms for three binary variables. Draw the truth table and express the Boolean function F(A,B,C) whose minterms are 1,3,5 ,7 as Canonica Sum of Minterms form.
   (b) Simplify the following Boolean functions to minimum number of literals:
      i. F = X'Y' + XYZ + X'Y
      ii. F = X + Y[Z + (X+Z)']
   (c) For the logic expression Y = AB' + A'B:
      i. Obtain the truth table.
      ii. Name the operation performed.
      iii. Realize this using AND, OR, NOT gates. [8+4+4]
3. Simplify the following Boolean expressions using K-map and implement them using NOR gates:
   (a) F (A, B, C, D) = AB'C' + AC + A'CD'
   (b) F (W, X, Y, Z) = W'X'Y'Z' + WXY'Z' + W'X'YZ + WXYZ. [16]
4. (a) Implement Full Adder using decoder and OR gates.
   (b) Realize the Boolean function T(X,Y,Z) = Σ(1,3,4,5) using logic gates for **hazard free**. [8+8]
5. (a) List the PLA programming table for the BCD to excess-3 code converter.
   (b) A ROM chip of 4,096 × 8 bits has two clip select inputs and operates from a 5-volt power supply. How many pins are needed for the integrated circuit package? Draw the block diagram of this ROM. [8+8]

6. (a) Draw the ckt diagram of 4 bit ring ring counter using D flipflops and explain its operation with the help of bit pattern.
   (b) Distinguish b/w transition table and excitation table? [16]

7. Explain the following related to sequential ckts with suitable examples.
   (a) State diagram
   (b) State table
   (c) State assignment. [16]

8. (a) For the given control state diagram obtain its equivalent ASM chart.
   (b) Design control logic circuit as shown in figure 8b using multiplexers. [8+8]

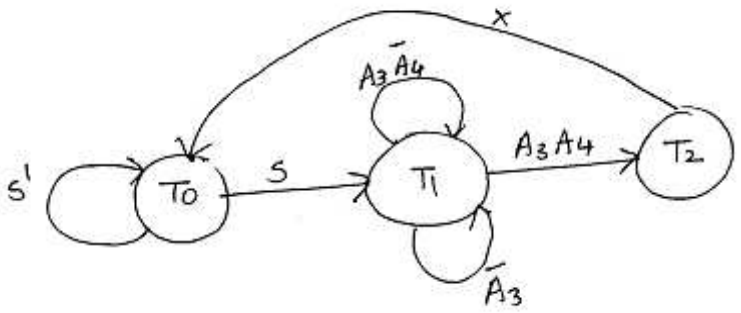

Figure 8b

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Code No: 07A3EC03 **Set No. 4**

II B.Tech I Semester Regular Examinations, November 2008
SWITCHING THEORY AND LOGIC DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the 7 bit Hamming code.
   (b) A receiver with even parity Hamming code is received the data as 1110110. Determine the correct code. [10+6]

2. (a) State and prove the following Boolean laws:
      i. Commutative
      ii. Associative
      iii. Distributive.
   (b) Find the complement of the following Boolean functions and reduce them to minimum number of literals:
      i. (bc'+ a'd) (ab' + cd')
      ii. b'd + a'bc' + acd + a'bc
   (c) Which gate can be used as parity checker? Why? [6+8+2]

3. (a) List the Boolean function simplification rules in the K-map
   (b) Simplify the following Boolean function for minimal SOP form using K-map and implement using NAND gates.
   F(W,X,Y,Z) = Σ(1,3,7,11,15) + d(0,2,5) [4+12]

4. Design a combinational circuit that converts a decimal digit from 2,4,2,1 code to 8, 4,-2,-1 code. [16]

5. (a) The following memory units are specified by the no of words times the number of bits per word. How many address lines and input-output data lines are needed in each case?
      i. 4K × 16
      ii. 2G × 8
      iii. 16M × 32
      iv. 256K × 64.
   (b) Give the number of bytes stored in the memories listed above. [16]

6. (a) Distinguish between a state table and a flow table?

(b) Draw the logic diagram and write functional table of an SR latch using NAND gates. Explain the operation. [16]

7. For the given minimal state - table:

(a) Give proper assignment.

(b) And design the circuit using D - Flip-flops. [6+10]

Present State	Next state,		out - put	
	X=0	X=1	X=0	X =1 (Z)
q_1	q_2	q_1	0	0
q_2	q_3	q_1	0	0
q_3	q_4	q_5	0	0
q_4	q_4	q_1	0	0
q_5	q_2	q_1	1	0

8. (a) How do you indicate moore outputs and mealy outputs in an ASM block.

(b) Obtain the ASM chart for the following state transition.
Start for State T_1; then if xy=00, go to T_2 if xy=01, go to T_3; if xy=10 go to T_1; otherwise go to T_3. [8+8]

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