Code No: R05310402 **Set No. 1**

III B.Tech I Semester Regular Examinations, November 2007
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) What are the parameters that are necessary to define the electrical characteristics of CMOS circuits? Mention the typical values of a CMOS NAND gate.
   (b) Design a CMOS 4-input AND-OR-INVERT gate. Draw the logic diagram and function table. [8+8]
2. (a) Mention the DC noise margin levels of ECL 10K family.
   (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case? [6+10]
3. (a) Write a VHDL Entity and Architecture for a 3-bit synchronous counter using Flip-Flops.
   (b) Explain the use of Packages. Give the syntax and structure of a package in VHDL. [8+8]
4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]
5. Design a 10 to 4 encoder with inputs 1- out of ?10 code and outputs in BCD? Provide the data flow style VHDL program? [16]
6. Write VHDL program for 1-bit comparator circuit with the input bits and equal, grater than and less than inputs from the previous stage and the outputs contain equal, greater than and less than conditions. Using this entity write VHDL program for 16-bit comparator using data flow style. Do not use any additional logic for this purpose. [16]
7. (a) Differentiate between ripple counter and synchronous counter? Design a 4-bit counter in both modes and estimate the propagation delay.
   (b) Design a modulo-88 counter using 74X163 Ics. [8+8]
8. (a) Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.
   (b) Determine the ROM size needed to realize the logic function performed by 74×153 and 74×139. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R05310402 **Set No. 2**

III B.Tech I Semester Regular Examinations, November 2007
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.
   (b) Analyze the fall time of CMOS inverter output with $R_L = 100\Omega, V_L = 2.5V$ *and* $C_L = 10PF$. Assume V_L as stable state voltage. [8+8]

2. (a) Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.
   (b) Explain sinking current and sourcing current of TTL output. Which of the above parameters decide the fan-out and how? [8+8]

3. (a) Write a VHDL Entity and Architecture for the following function?

$$F(x) = a \oplus b \oplus c$$

   Also draw the relevant logic diagram.
   (b) Explain the use of Packages Give the syntax and structure of a package in VHDL [8+8]

4. Design the logic circuit and write a data-flow style VHDL program for the following functions.
   (a) $F(X) = \Sigma_{A,B,C,D}\,(0, 2, 5, 7, 8, 10, 13, 15) + d\,(1, 6, 11)$
   (b) $F(Y) = \Pi_{A,B,C,D}\,(1, 4, 5, 7, 9, 11, 12, 13, 15))$ [8+8]

5. With the help of logic diagram explain 74×157 multiplexer? Write the data flow style VHDL program for this IC? [16]

6. Design a 24-bit comparator circuit using 74×682 ICs and discuss the functionality of the circuit. Also implement VHDL source code in data flow style. [16]

7. (a) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table.
   (b) Design a Modulo-12 ripple counter using 74×74? Write a VHDL program for this logic using data flow style. [8+8]

8. (a) Discuss how PROM, EPROM and EEPROM technologies differ from each other.

(b) With the help of timing waveforms, explain read and write operations of SRAM. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R05310402 **Set No. 3**

III B.Tech I Semester Regular Examinations, November 2007
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the operation of the circuit diagram.
   (b) Design a CMOS transistor circuit that has the functional behavior as

$$f(x) = \overline{(a + \overline{b})\ (b\ +\ c)(a + \overline{c})}$$

   Also draw the relevant circuit diagrams. [8+8]

2. (a) Explain the following terms with reference to TTL gate.
      i. Voltage levels for logic '1' & logic '0'
      ii. DC Noise margin
      iii. Low-state unit load
      iv. High-state fan-out
   (b) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table. [8+8]

3. Explain with an example the syntax and the function of the following VHDL statements.
   (a) Process statement
   (b) If, else and elseif statements
   (c) Case statement
   (d) Loop statement [4×4=16]

4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]

5. (a) It is necessary to identify the position of mechanical disk, when rotates with a step of 45^0. Give the necessary encoding mechanism and draw the logic circuit?
   (b) Using two 74×138 decoders design a 4 to 16 decoder. [16]

6. (a) Write a VHDL program for the circuit that counts number of Ones in a 16-bit register using structural style of modeling.
   (b) Design a 4×4 combinational multiplier and the write the necessary VHDL program data flow model. [8+8]

7. Show the logic diagram of 74×175 IC and write VHDL program for this IC in data flow style. Using this entity develop the program for 16-bit register and show the corresponding circuit also explain how the register is cleared? [16]

8. (a) Draw the basic cell structure of Dynamic RAM. What is the necessity of refresh cycle? Explain the timing requirements of refresh operation.

   (b) Discuss in detail ROM access mechanism with the help of timing waveforms. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆

Code No: R05310402 **Set No. 4**

III B.Tech I Semester Regular Examinations, November 2007
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the operation of the circuit diagram.
   (b) Design a CMOS transistor circuit that has the functional behavior as

$$f(x) = \overline{(\mathrm{a} + \overline{\mathrm{b}})\ (\mathrm{b}\ +\ \mathrm{c})(\mathrm{a} + \overline{\mathrm{c}})}$$

   Also draw the relevant circuit diagrams. [8+8]

2. (a) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.
   (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case? [8+8]

3. (a) Explain the various data types supported by VHDL. Give the necessary examples.
   (b) Discuss the case statement and its use in the VHDL program. [8+8]

4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]

5. Design a two-digit BCD adder with logic gates. Using this logic write the VHDL program. In structural style of modeling. [8+8]

6. Design a combinational logic circuit that counts the number of ones in a 24-bit register. Write a VHDL program for the same using structural style or modeling. [16]

7. (a) Draw the logic diagram of 74×163 binary counter and explain its operation.
   (b) Design a modulo-100 counter using two 74×163 binary counters? [8+8]

8. (a) Design an 8×4 diode ROM using 74×138 for the following data starting from the first location.

$$6, 9, 0, C, D, 1, F, D$$

   (b) How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and two's complement overflow output. Show the block schematic with all inputs and outputs. [8+8]

⋆ ⋆ ⋆ ⋆ ⋆