Code No: R05310402 **Set No. 1**

III B.Tech I Semester Supplimentary Examinations, February 2008
DIGITAL IC APPLICATIONS
(Common to Electronics & Communication Engineering and Electronics & Instrumentation Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the following terms with reference to CMOS logic.
   i. Logic Levels
   ii. Noise margin
   iii. Power supply rails
   iv. Propagation delay
   (b) What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic. [8+8]
2. (a) Draw the circuit diagram of two-input 10K ECL OR gate and explain its operation.
   (b) List out different categories of characteristics in a TTL data sheet. Discuss electrical and switching characteristics of 74LS00. [8+8]
3. (a) Discuss the steps in VHDL design flow.
   (b) Explain the difference in program structure of VHDL and any other procedural language. Give an example. [8+8]
4. (a) Design a logic circuit to detect prime number of a 4-bit input? Write the VHDL program for the same in structural style of modelling.
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function? [8+8]

$$F(X) = \Sigma_{A,B,C,D}\,(3, 5, 6, 7, 10, 13, 14) + d\,(1, 2, 4, 15)$$

5. Design a 3 input 5-bit multiplexer. Write the truth table and draw the logic diagram. Provide the data flow VHDL program for the same. [16]
6. A simple floating-point encoder converts 16-bit fixed-point data using four high order bits beginning with MSB. Design the logic circuit and write VHDL data-flow program. [16]
7. (a) Design a 4-bit binary synchronous counter using 74×74. Write VHDL program for this logic. Using data flow style.
   (b) Design a modulo-60 counter using 74×163 Ics. [8+8]
8. (a) Discuss how PROM, EPROM and EEPROM technologies differ from each other.

(b) With the help of timing waveforms, explain read and write operations of SRAM. [8+8]

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Code No: R05310402 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain the following terms with reference to CMOS logic.
   i. Logic Levels
   ii. Noise margin
   iii. Power supply rails
   iv. Propagation delay
   (b) What is the difference between transmission time and propagation delay? Explain these two parameters with reference to CMOS logic. [8+8]

2. (a) Mention the DC noise margin levels of ECL 10K family.
   (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case? [6+10]

3. (a) Write a VHDL Entity and Architecture for the following function?

$$\mathrm{F(x)} = \mathrm{a} \oplus \mathrm{b} \oplus \mathrm{c}$$

   Also draw the relevant logic diagram.
   (b) Explain the use of Packages Give the syntax and structure of a package in VHDL [8+8]

4. Design the logic circuit and write a data-flow style VHDL program for the following functions?
   (a) $F(A) = \Pi_{p,q,r,s}\,(1,3,4,5,6,7,9,12,13,14)$
   (b) $F\,(X) = \Sigma_{A,B,C,D}\,(3,5,6,7,13) + d\,(1,2,4,12,15)$ [8+8]

5. (a) Design a 32 to 1 multiplexer using four 74×151 multiplexers and 74X139 decoder.
   (b) Realize the following expression using 74×151 IC [8+8]

$$f(Y) = AB + BC + AC$$

6. Write VHDL program for 8-bit comparator circuit. Using this entity write VHDL program for 24-bit comparator. Show the additional logic used for this purpose use structural style or modeling. [16]

7. (a) Design a modulo-8 binary counter and decoder with glitch-free outputs. Explain the operation.
   (b) Design a modulo-100 counter using two 74X163 binary counters. [8+8]

8. (a) Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation.
   (b) Design an 8×8 diode ROM using 74×138 for the following data starting from the first location. [8+8]

$$11, 22, 33, FF, DD, CC, 01, 7E$$

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Code No: R05310402 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Design CMOS transistor circuit for 2-input AND gate. Explain the circuit with the help of function table?
   (b) Draw the resistive model of a CMOS inverter circuit and explain its behavior for LOW and HIGH outputs. [8+8]
2. (a) Design a three input NAND gate using diode logic and a transistor inverter? Analyze the circuit with the help of transfer characteristics.
   (b) Explain sinking current and sourcing current of TTL output? Which of the parameters decide the fan-out and how? [8+8]
3. (a) Write a VHDL Entity and Architecture for the following function?

$$F(x) = a \oplus b \oplus c$$

   Also draw the relevant logic diagram.
   (b) Explain the use of Packages Give the syntax and structure of a package in VHDL [8+8]
4. (a) Explain data-flow design elements of VHDL.
   (b) Write a Behavioral style VHDL program for the following functions. [8+8]

$$F(S) = A \oplus B \oplus C_1$$
$$F(C_O) = AB + AC_1 + BC_1$$

5. (a) Design a 32 to 1 multiplexer using four 74×151 multiplexers and 74X139 decoder.
   (b) Realize the following expression using 74×151 IC [8+8]

$$f(Y) = AB + BC + AC$$

6. Write VHDL program for 1-bit comparator circuit with the input bits and equal, grater than and less than inputs from the previous stage and the outputs contain equal, greater than and less than conditions. Using this entity write VHDL program for 16-bit comparator using data flow style. Do not use any additional logic for this purpose. [16]
7. (a) Design a switch debouncer circuit using 74×109 IC. Explain the operation using timing diagram.

(b) Discuss the logic circuit of 74×377 register. Write a VHDL program for the same in structural style. [8+8]

8. (a) Realize the logic function performed by 74×381 with ROM.

(b) How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and two's complement overflow output. Show the block schematic with all inputs and outputs. [8+8]

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Code No: R05310402 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain how to estimate sinking current for low output and sourcing current for high output of CMOS gate.
   (b) Analyze the fall time of CMOS inverter output with $R_L = 100\Omega, V_L = 2.5V$ *and* $C_L = 10PF$. Assume V_L as stable state voltage. [8+8]

2. (a) Design a TTL three-state NAND gate and explain the operation with the help of function table.
   (b) Explain the following terms with reference to TTL gate.
      i. Voltage levels for logic '1' & logic '0'
      ii. DC Noise margin
      iii. Low-state unit load
      iv. High-state fan-out [8+8]

3. (a) Write a VHDL Entity and Architecture for a 3-bit synchronous counter using Flip-Flops.
   (b) Explain the use of Packages. Give the syntax and structure of a package in VHDL. [8+8]

4. (a) Explain structural design elements of VHDL.
   (b) Design the logic circuit and write a data-flow style VHDL program for the following function. [8+8]

$$F(R) = \Pi_{A,B,C,D}(1, 4, 5, 7, 9, 13, 15)$$

5. (a) Using two 74×138 decoders design a 4 to 16 decoder?
   (b) Realize the following expression using 74×151 IC? [16]

$$f(X) = \overline{A}BC + A\overline{B}C + AB\overline{C}$$

6. (a) Design a 16-bit comparator using 74×85 ICs.
   (b) Write a behavioral VHDL program to compare 16-bit signed and unsigned integers . [16]

7. (a) Draw the logic diagram of 74×163 binary counter and explain its operation.
   (b) Design a modulo-100 counter using two 74×163 binary counters? [8+8]

8. (a) Explain the internal structure of 64K×1 DRAM. With the help of timing waveforms discuss DRAM access.

   (b) Explain the necessity of two-dimensional decoding mechanism in memories. Draw MOS transistor memory cell in ROM and explain the operation. [8+8]

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