Code No : 9A10504/R09

B.Tech. III Year II Semester Regular & Supplementary Examinations

Set-1

April/May - 2013

LINEAR AND DIGITAL IC APPLICATIONS

(Common to EEE and MCT)

Time: 3 Hours | Max. Marks: 70

*Answer any **FIVE** Questions*

*All Questions carry **Equal** Marks*

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1. (a) List out different configurations of differential amplifier.
   (b) Compare and contrast an ideal op-amp and practical op-amp.
   (c) List out the AC characteristics of an op-amp and discuss about them.

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2. (a) Design a differentiator to differentiate an input signal that varies in frequency from 10 Hz to about 1 kHz. If a sine wave of 1 V peak at 1000 Hz is applied to this differentiator draw the output waveforms.
   (b) Design a logarithmic amplifier for positive input voltages in the range 5 mV to 50 V.

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3. (a) Draw the block schematic of a PLL describing the function of each block briefly.
   (b) Explain the different applications of PLL.

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4. (a) Design a 4-input CMOS AND-OR-INVERT gate. Draw the logic diagram and function table.
   (b) Distinguish between static and dynamic power dissipation of a CMOS circuit.

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5. (a) Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin propagation delay and fan-out.
   (b) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.

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6. (a) Explain structural design elements of VHDL.
   (b) Explain with example the syntax and the function of the following VHDL statements,
      (i) Concurrent signal assignment statement
      (ii) Selected signal assignment statement
      (iii) Port map.

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7. (a) Using two 74 × 138 decoders design a 4 to 16 decoder.
   (b) Write a data flow style VHDL program for the above design.

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8. (a) Explain working of the various programmable logic devices.
   (b) Differentiate between ripple counter and synchronous counter. Design a 4-bit counter in both modes and estimate the propagation delay.