Code No: R09220501 **R09** **Set No. 2**

II B.Tech II Semester Examinations,APRIL 2011
COMPUTER ORGANIZATION
Common to Chemical Engineering, Computer Science And Engineering
Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate between microprogramming and nanoprogramming.
   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [7+8]
2. What are the different types of Mapping Techniques used in the usage of Cache Memory? Explain. [15]
3. (a) Draw a flowchart to explain how addition and subtraction of two fixed point numbers can be done. Also, draw a circuit using full adders for the same.
   (b) Explain Booth's logorithm with its theoretical basis. [7+8]
4. (a) Draw the block diagram of a computer system and describe each of its parts along with their functions. Also designate the information flow between the parts with arrows.
   (b) Explain the term 'memory bus bottleneck'.
   (c) Distinguish between multiprocessor and a multicomputer. [5+5+5]
5. Explain the following:
   (a) Asynchronous Serial Transfer
   (b) Asynchronous Communication Interface. [7+8]
6. (a) What is meant by arithmetic pipeline? Explain.
   (b) Explain pipeline for floating point addition and subtraction. [7+8]
7. (a) Explain commonly employed bit shift operators such as shift left, right, circular shift left/right and arithmetic shift left/right. Give 8-bit examples.
   (b) Design a circuit for combined shift left/right operations. Assume register length is 4 bits and employ RS flip-flops. [10+5]
8. (a) Explain multiport memory organization with a neat sketch.
   (b) Explain system bus structure for multiprocessors with a neat sketch. [7+8]

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Code No: R09220501 **R09** **Set No. 4**

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Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
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1. (a) How many bits are needed to store the result addition, subtraction, multiplication and division of two n-bit unsigned numbers. Prove.
   (b) What is overflow and underflow? What is the reason? If the computer is considered as infinite system do we still have these problems. [7+8]

2. (a) Design a circuit transferring data from a 4bit register which uses D flip-flops to another register which employs RS flip-flops.
   (b) What are register transfer logic languages? Explain few RTL statement for branching with their actual functioning. [7+8]

3. Draw the general block diagram of a microsequencer. Explain clearly the inputs and outputs of the same along with their functioning. [15]

4. (a) Explain bit oriented and character oriented protocols in serial communication.
   (b) What are the different issues behind serial communication? Explain. [7+8]

5. (a) Find out what are the actual values of the following IEEE 754 single precision number.
      i. Sign=0, exponent=all 1s and fraction field is not 0.
      ii. Sign=0, exponent=all 0s and fraction field is 0.
      iii. Sign=1, exponent=all 1s and fraction field is 0.
      iv. Sign=0, exponent=1000 0001, fraction=1100 0000 0000 0000 0000 000
   (b) Why is bus arbitration required. Discuss about any two bus arbitration methods. [10+5]

6. (a) Explain how Flynn classified the processors into different streams by giving an example for each stream.
   (b) Explain tightly coupled and loosely coupled systems with suitable examples. [7+8]

7. Explain the following in related with Vector Processing
   (a) Super Computers
   (b) Vector operations
   (c) Matrix multiplication
   (d) Memory interleaving. [4+3+4+4]

8. (a) A two-way set associative cache memory uses blocks of 4 words. The cache can accommodate a total of 2048 words from main memory. The main memory size is 124K × 32
   i. Formulate the information required to construct cache Memory.
   ii. What is the size of cache Memory?

   (b) The access time of cache memory is 100ns and that of main memory is 1000ns. It is estimated that 80% of memory requests are for read and the remaining 20% for write. The hit ratio for read access only is 0.9. A write through procedure is used.
   i. What is the average access time of the system considering only read cycles?
   ii. What is the average access time of the system considering both read and write cycles? [7+8]

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Code No: R09220501 **R09** **Set No. 1**

II B.Tech II Semester Examinations,APRIL 2011
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Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Explain RISC pipeline in detail.
   (b) Explain vector processing. [7+8]
2. Draw circuit for BCD addition and subtraction. Explain its functionality with mathematical background. [15]
3. (a) Explain the working of 8 × 8 Omega Switching network.
   (b) Explain the functioning of Binary Tree network with 2 × 2 Switches. Show a neat sketch. [7+8]
4. (a) What are the different types of I/O communication techniques? Give brief notes.
   (b) In the above techniques, which is the most efficient? Justify your answer.[7+8]
5. (a) Explain the variety of techniques available for sequencing of microinstructions based on the format of the address information in the microinstruction.
   (b) Hardwired control unit is faster than microprogammed control unit. Justify this statement. [7+8]
6. (a) If cache access time is 70 ns, memory access time is 700ns.
      i. Compute the formula for average access time.
      ii. Compute hit and miss ratios if the average access time is 140ns.
   (b) What is RAID? What are the advantages of using this technique.
   (c) Show the memory hierarchy and give the brief explanation. [6+5+4]
7. What do you mean by instruction set architecture (ISA). What is the completeness and orthogonality with respect to ISA. What are the design issues related to ISA? [15]
8. (a) Find the actual number from its IEEE 754 representation.
   Sign = 0
   Exponent = 1000 0000
   Mantissa = 1100 0000 0000 0000 0000 000
   (b) What is meant by normalization in floating point representation? Why do we need it? What is bias? What normalization is used in IEEE 754 standard? [5+10]

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Code No: R09220501 **R09** **Set No. 3**

II B.Tech II Semester Examinations,APRIL 2011
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Time: 3 hours **Max Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Differentiate I/O Bus and memory Bus.
   (b) What are major functional differences between memory mapped I/O and Isolated I/O. [7+8]
2. What is paging? Explain how the technique of paging can be implemented. [15]
3. (a) Explain nanoinstructions and nanometry. Why do we need them?
   (b) Describe advantages and disadvantages of horizontal and vertical microcoded systems. [7+8]
4. (a) Distinguish between high level and low level languages?. What are the requirements for a good programming language?
   (b) Explain with an example IEEE 754 representation for single precision and double precision floating point numbers. [10+5]
5. Write short notes on the following:
   (a) RISC pipeline
   (b) Vector processing
   (c) Array processors. [5+5+5]
6. (a) Represent two n-bit unsigned numbers multiplications with a series of n/2-bit multiplications.
   (b) Explain single precision and double precision calculations. In general how many bytes are used for both and what is the precision we get. Give some examples where double precision calculations are needed. [7+8]
7. (a) What are the different physical forms available to establish an inter-connection network? Give the summary of those.
   (b) Explain time-shared common bus Organization.
   (c) Explain system bus structure for multiprocessors. [5+5+5]
8. There exists three 4-bit registers (A,B, and C) and 4-bit data lines (say D). Design a circuit to transfer data from any register to any other register including data lines and vice versa. [15]

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