Code No: R059210202 **Set No. 1**

II B.Tech I Semester Regular Examinations, November 2007
PULSE AND DIGITAL CIRCUITS
(Common to Electrical & Electronic Engineering, Electronics & Communication Engineering, Electronics & Instrumentation Engineering and Electronics & Telematics)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Prove that an RC circuit behaves as a reasonably good integrator if RC > 15T, Where T is the period of an input '$E_m \sin \omega t$'.
   (b) What is the ratio of the rise time of the three sections in cascade to the rise time of Single section of low pass RC circuit. [8+8]

2. (a) Draw the circuit diagram of slicer circuit using Zener diodes and explain its operation with the help of its transfer characteristic.
   (b) Draw the circuit diagram of emitter coupled clipper. Draw its transfer characteristics indicating all intercepts, slopes and voltage levels derive the necessary equations. [8+8]

3. (a) Explain the terms pertaining to transistor switching characteristics.
      i. Rise time.
      ii. Delay time.
      iii. Turn-on time.
      iv. Storage time.
      v. Fall time.
      vi. Turn-off time.
   (b) Give the expression for risetime and falltime in terms of transistor parameters and operating currents. [6+10]

4. In the nonsaturated binary shown in figure 4, the avalanche diodes D1 and D2 are nominally identical, as are diodes D3 and D4. The breakdown voltage V?Z of D3 and D4 is larger than the breakdown voltage V_Z of D1 and D2. Verify that the transistors do not enter the saturation region. Assume that D3 and D4 are always in the breakdown region and that either D1 or D2 but not both, is in the breakdown region. Then verify these assumptions. [16]

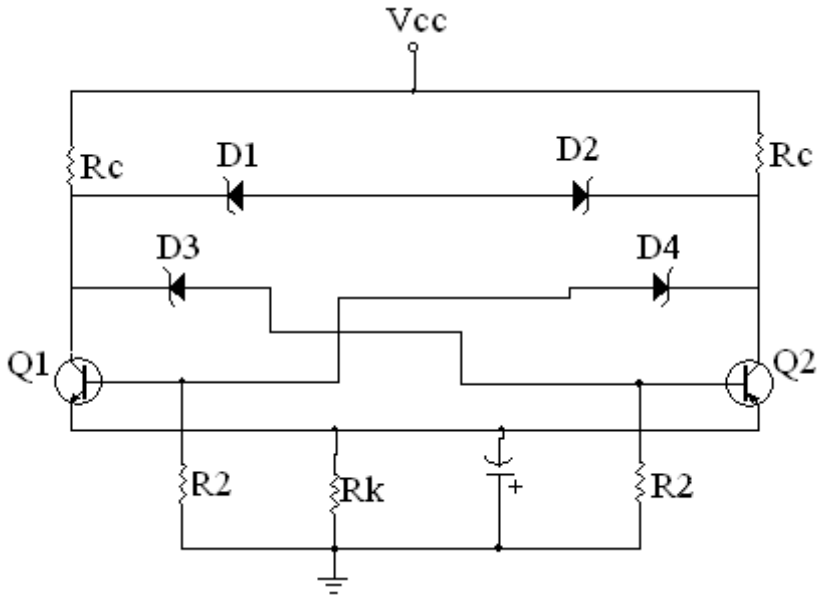

Figure 4

5. (a) Draw and clearly indicate the restoration time and flyback time on the typical waveform of a time base voltage.
   (b) Derive the relation between the slope, transmission and displacement errors
   (c) Explain how UJT is used for sweep circuit? [6+4+6]

6. (a) What do you mean by synchronization ?
   (b) What is the condition to be met for pulse synchronization?
   (c) Compare sine wave synchronization with pulse synchronization? [4+6+6]

7. (a) Why are sampling gates called Selection circuits?
   (b) What are the advantages of unidirectional sampling gates?
   (c) What are the applications of sampling gates? [6+4+6]

8. (a) With the help of circuit diagram explain the purpose of clamping diode in a positive diode AND gate.
   (b) Explain the effect of and diode capacitance on the output pulse of diode AND gate. [8+8]

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Code No: R059210202 **Set No. 2**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

⋆ ⋆ ⋆ ⋆ ⋆

1. (a) Prove that an RC circuit behaves as a reasonably good integrator if RC > 15T, Where T is the period of an input '$E_m \sin \omega t$'.
   (b) What is the ratio of the rise time of the three sections in cascade to the rise time of Single section of low pass RC circuit. [8+8]

2. (a) State and prove clamping -circuit theorem.
   (b) A clamping circuit and input wave form is shown in figure 2b calculate and plot to scale the steady state output [8+8]

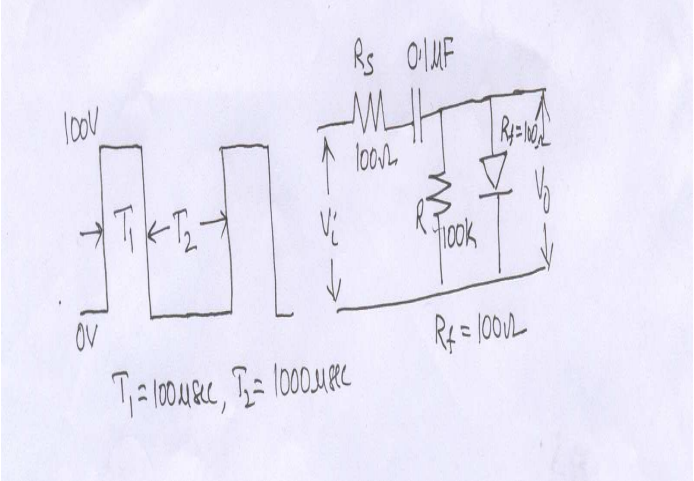

Figure 2b

3. Write Short notes on:
   (a) Diode switching times
   (b) Switching characteristics of transistors
   (c) FET as a switch. [4+8+4]

4. (a) Consider the symmetrical emitter triggering circuit of the figure 4 with Rc=3Re, R_1=2R2, and V_{CC}=6V. Indicate all the circuit voltages in the quiescent state and indicate also the voltages immediately after a 5-V positive step is applied. Assume that D3 and D4 are always in the breakdown region and that either D1 or D2 but not both in the breakdown region.

(b) Repeat part (a) for a 25-V step. What limits the maximum size of the input step? What limits the minimum size of the input step? [16]

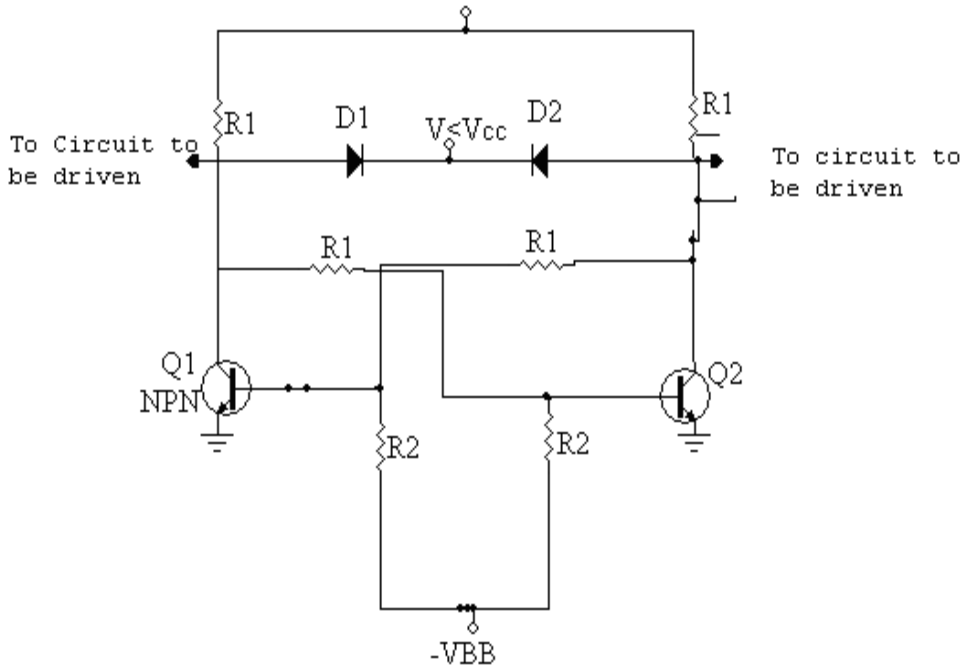

Figure 4

5. (a) Draw and clearly indicate the restoration time and flyback time on the typical waveform of a time base voltage.
   (b) Derive the relation between the slope, transmission and displacement errors
   (c) Explain how UJT is used for sweep circuit? [6+4+6]

6. (a) Explain the factors which influence the stability of a relaxation divider with the help of a neat waveforms.
   (b) A UJT sweep operates with Vv = 3V, Vp=16V and η=0.5. A sinusoidal synchronizing voltage of 2V peak is applied between bases and the natural frequency of the sweep is 1kHz, over what range of sync signal frequency will the sweep remain in 1:1 synchronism with the sync signal? [8+8]

7. (a) What is sampling gate? Explain how it differ from Logic gates?
   (b) What is pedestal? How it effects the output of a sampling gates?
   (c) What are the drawbacks of two diode sampling gate? [6+6+4]

8. (a) Draw and explain the circuit diagram of integrated positive RTL NOR gate
   (b) Compare the RTL and DTL logic families in terms of Fan out, propagation delay, power dissipated per gate and noise immunity. [8+8]

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Code No: R059210202 **Set No. 3**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) Verify $V_2 = (V/2)(e^{2x}-1)/(e^{2x}+1) = (V/2)$ tanhx for a symmetrical square wave applied to a low pass RC circuit.
   (b) Derive the expression for percentage tilt(P) of a square wave output of RC high pass circuit. [8+8]
2. (a) Give the circuits of different types of shunt clippers and explain their operation with the help of their transfer characteristics.
   (b) Draw the diode differentiator comparator circuit and explain the operation of it when ramp input signal is applied. [8+8]
3. Write Short notes on:
   (a) Diode switching times
   (b) Switching characteristics of transistors
   (c) FET as a switch. [4+8+4]
4. (a) Draw the circuit diagram of a Schmitt trigger circuit and explain its operation. Derive the Expressions for its UTP and LTP.
   (b) Explain how an Schmitt trigger circuit acts as a comparator. [12+4]
5. (a) Explain the basic principles of Miller and bootstrap time base generators.
   (b) A transistor bootstrap ramp generator is to produce a 15V, 5ms output to a 2kohms load resistor. The ramp is to be linear within 2%. Design a suitable circuit using V_{cc} = 22V, $-V_{EE}$ = -22V and transistor with $h_{fe(min)} = 25$. The input pulse has an amplitude of -5V, pulse width = 5ms and space width = 2.5ms. [8+8]
6. (a) What is relaxation oscillator? Name some negative resistance devices used as relaxation oscillators and give its applications.
   (b) With the help of a circuit diagram and waveforms, explain the frequency division by an astable multivibrator? [8+8]
7. (a) Why are sampling gates called linear gates?
   (b) What are the other names of a gate signal?
   (c) Compare the unidirectional and bi-directional sampling gates. [6+4+6]

8. (a) Why totem pole is used in DTL? Draw the circuit diagram and explain a DTL gate with this.
   (b) Verify the truth table of RTL NOR gate with the circuit diagram of two inputs. [8+8]

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Code No: R059210202 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
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1. (a) What is the function of a comparator? Explain its operation.
   (b) Explain the response of a low pass circuit to an exponential input is applied.
   (c) Explain the response of RL circuit when a rectangular pulse is applied [4+6+6]

2. (a) For the circuit shown in figure 2a , V_i is a sinusoidal voltage of peak 100 volts. Assume ideal diodes. Sketch one cycle of output voltage. Determine the maximum diode Current.

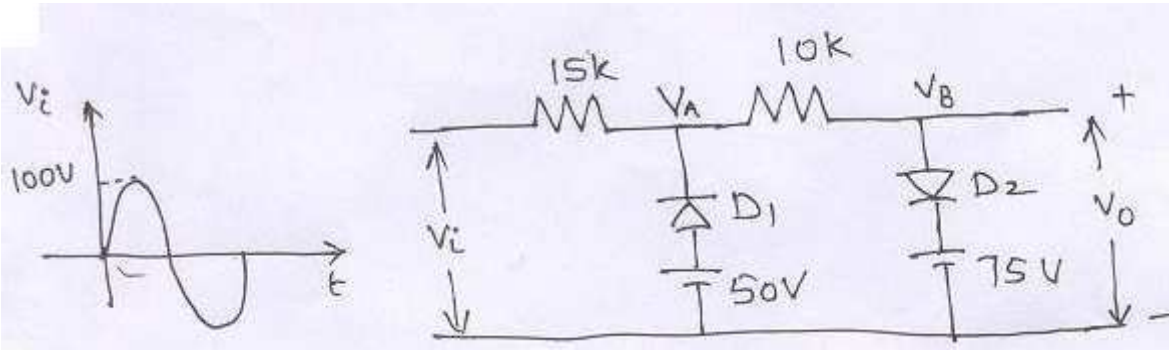

Figure 2a

   (b) Explain positive peak clipping with reference voltage. [12+4]

3. Write Short notes on:
   (a) Diode switching times
   (b) Switching characteristics of transistors
   (c) FET as a switch. [4+8+4]

4. In the monostable circuit of the given figure 4 the resistor R is connected to an auxiliary supply V_1 instead of V_{YY}. If A2 is in saturation or clamp and if A1 is OFF in the stable state, verify that the gate time T is given by Eq. $T = \tau \ln(V_{YY}+I_1R_Y-V\sigma)/(V_{YY}-V\gamma)$ with V_{YY} replaced by V_1. [16]

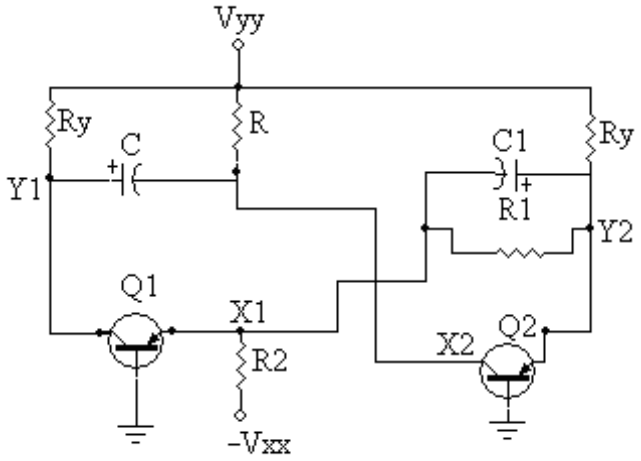

Figure 4

5. (a) How are linearly varying current waveforms generated?

   (b) In the boot strap circuit shown in figure5 V_{cc} = 25 V, V_{EE} = -15 V, R = 10 K ohms, R_B = 150 K ohms, C = 0.05 μF. The gating waveform has a duration of 300 μs. The transistor parameters are h_{ie} = 1.1Kohms, h_{re} = 2.5 x 10^{-4} K ohmsh_{fe} =50 h_{oe} = 1/40K ohms.

   i. Draw the waveform of IC1 and Vo , labeling all current and voltage levels,

   ii. What is the slope error of the sweep?

   iii. What is the sweep speed and the maximum value of the sweep voltage?

   iv. What is the retrace time Tr for C to discharge completely?

   v. Calculate the recovery time T1 for C1 to recharge completely. [6+10]

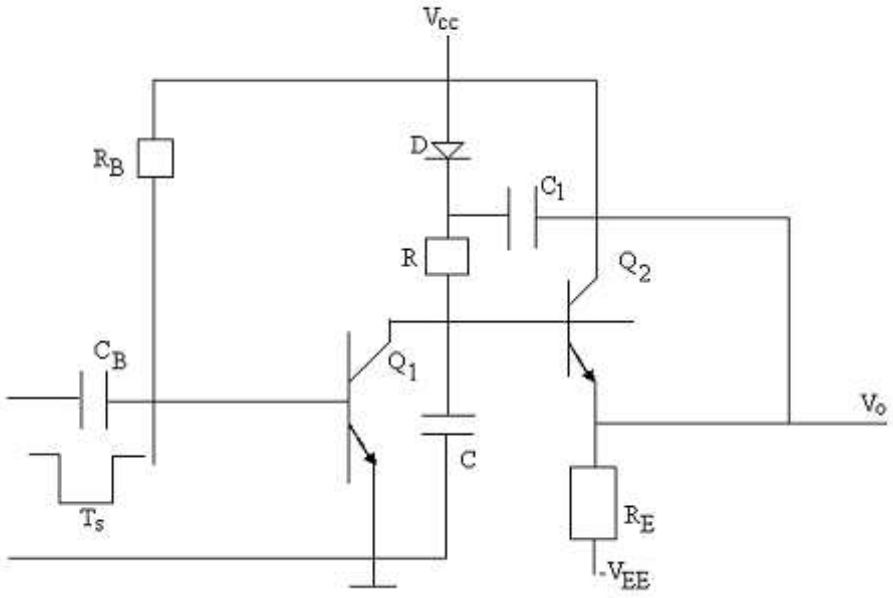

Figure 5

6. (a) Explain how monostable multivibrator is used as frequency divider?
   (b) Draw and explain the block diagram of frequency divider without phase jitter. [8+8]

7. (a) Why are sampling gates called linear gates?
   (b) What are the other names of a gate signal?
   (c) Compare the unidirectional and bi-directional sampling gates. [6+4+6]

8. (a) What are the basic logic gates which perform almost all the operations in Digital communication systems.
   (b) Give some applications of logic gates.
   (c) Define a positive and negative logic systems.
   (d) Draw a pulse train representing a 11010111 in a synchronous positive logic digital system. [4+4+4+4]

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